Analysis of a Multiple Cell Upset Failure Model for Memories

Sanghyeon Baeg, Pedro Reviriego, Juan Antonio Maestro, ShiJie Wen, and Richard Wong

Abstract— **As technology shrinks, Multiple Cell Upsets (MCU) are becoming a more prominent effect with a large impact on memory reliability. The use of single error correction codes (SEC) and interleaving is the most common approach to protect memories from MCUs. In the last years several models have been proposed to evaluate reliability of memories that use SEC and interleaving in the presence of MCUs. In a recent paper some of the authors proposed an analytical model for the failure probability of a memory suffering MCUs. In this paper the analytical model is first validated by simulation showing a good agreement between the model and simulation experiments based on the model assumptions. Then the effects of some constraints imposed in derivation of the model are evaluated by comparing the model results with simulations experiments on which those constraints are removed. This comparison illustrates the accuracy of the model and can be useful for designers that plan to use the model to evaluate memory reliability.**

Index Terms— **Interleaving distance, Soft error, MCU, Scrubbing, Compound-Poisson**

I. Introduction

Computer memories are sensitive to soft errors which can affect system reliability. Memory cells can be disturbed by high-energy neutron particles from terrestrial atmosphere or alpha particles resulted from IC package material. Previous studies showed soft error rate is closely related to critical charge [1], [2] and process [3], [4]. Therefore a natural way to mitigate soft error issues is to increase critical charge at state nodes, or to use process related immunity techniques such as well and substrate engineering. Another option is to include error correction capabilities on the memory so that some of the errors can be corrected. This is normally done by using a single error correction (SEC) code on each memory word so that single errors in a word can be corrected [5]. Scrubbing can be combined with single error correction to further increase reliability by periodically reading the memory and correcting the single errors so that they do not accumulate over time [6]. The combination of SEC and scrubbing is effective against single event upsets but not against MCUs as the errors in an MCU tend to be physically close and therefore it is likely that they affect more than one bit of the same memory word. To deal with MCUs interleaving is commonly used [5]. Interleaving ensures that cells that belong to the same word are physically apart so that only one can be affected by errors in the same MCU.

In [7] an analytical model to calculate the failure probability of a memory affected by MCUs that incorporates SEC and interleaving was presented. This model provides a conservative estimate of the reliability of the memory and can be used at the design stage to check that the memory will meet a given reliability level. The objective of this paper is to first validate the model with simulation experiments that are done with the same assumptions used in the derivation. A second goal is to compare the results obtained with the model with simulation experiments on which some of the constraints used in the derivation are removed. This comparison will help in understanding how conservative the model is in different situations.

The rest of this paper is organized as follows. Section II briefly reviews the analytical model discussing the assumptions used in its derivation. The validation of the model by simulation is done in Section III. Section IV discusses the accuracy of the model in different situations, and Section V concludes the paper.

II. SRAM Failure Model

In this section the analytical model presented in [7] is reviewed. The memory configuration is as follows, each word in the SRAM is protected by a SEC code and interleaving is such that errors in an MCU always fall on cells that belong to different words. If an SRAM with M memory cells with W words and B bits per word is assumed, the values will depend on the interleaving distance (ID) as shown in (1). W_N (B_N) is the number of words (bits per words) when ID is N. That is the word-length will decrease as the ID increases.

Sanghyeon Baeg is with the School of Electrical Engineering and Computer Science, Hanyang University, 1271 Sa1-Dong Sangrok-Gu Ansan, Kyung-Gi-Do, Korea (phone/fax: +82-31-400-5237; e-mail: bau@hanyang.ac.kr).

Pedro Reviriego and Juan Antonio Maestro are with Universidad Antonio de Nebrija, C/ Pirineos, 55 E-28040 - Madrid, Spain (phone: +34 914521100; fax: +34 914521110; email: {previrie ,jmaestro}@nebrija.es).

ShiJie Wen, and Richard Wong are with the Component Engineering Group at Cisco Systems Inc. 170 W. Tasman Dr. San Jose CA 95134, U.S.A. (e-mail: shwen@cisco.com, rickwon@cisco.com).

This research was supported by the Ministry of Knowledge Economy Korea under the Information Technology Research Center support program supervised by the Institute for Information Technology Advancement under Grant IITA-2008-C1090-0804-0009, the Spanish Ministry of Science and Innovation under Grant ESP-2006-04163, and the Regional Government of Madrid and the European Union FEDER programme.

$$M = W_{ID} \cdot B_{ID}$$
$$W_{ID} = W_1 \cdot ID \quad (1)$$
$$B_{ID} = \frac{B_1}{ID}$$

Then, the reliability of a device, *R(t)*, can be expressed in terms of failing probability, *F(t)*, as shown in "(2),"

$$R(t) = 1 - F(t) \quad (2)$$
$$F(t) = \sum_{X=1}^{\infty} P(X,t) P_f(X)$$

where P(X,t) is defined as the probability of having *X* number of upsets in a device at time *t*. $P_f(X)$ in "(2)" is the failing probability when there are *X* number of upsets in a memory. The Poisson process is typically used to model random events. However, the process does not correctly model the MCU cases, which can have multiple upsets per event [8], [9]. To model MCU effects, the compound Poisson (CP) model is used to express the probability of P(X,t). The CP model has a Poisson parameter, λ, and the parameters for the compounding distribution. When the compounding distribution is *f(x)*, the CP model can be expressed as "(3)" [8]. f^{Y*} is Y fold convolutions of *f(x)*.

$$P(X,t) = \sum_{Y=0}^{\infty} \frac{(\lambda t)^Y e^{-\lambda t}}{Y!} f^{Y^*}(X);\ X = 0,1,2...;\ \lambda > 0 \quad (3)$$

Geometric distribution was used to model grouped arrivals [8][10] and the MCU effect [5]. The similarity between the geometric distribution and test results was observed and used in the experimental results in [7]. "(4)" shows the CP geometric model that used geometric distribution, $f(x) = (1-r)r^{x-1}$ as a compounding distribution, where "*r*" is the geometric parameter. Details of the geometric CP model have been previously discussed in [8]. The vertical double-numbers in parentheses denote combinatorial notation.

$$P(X,t) = \sum_{Y=1}^{X} \frac{(\lambda t)^Y e^{-\lambda t}}{Y!} \binom{X-1}{Y-1} r^{X-Y} (1-r)^Y \quad (4)$$

As discussed before in the probability calculations, it is assumed that each word is protected by SEC. P_f in "(5)" shows the probability of *X* upsets landing on *L* cells with at least two upset cells in the same word.

$$P_f(X) = \sum_{L=2}^{X} G_L \cdot {}_L T_X \cdot \left(\frac{1}{M}\right)^X \quad (5)$$

G_L is the number of cell groups with L members that can cause a failure. Each group is established by selecting L from *M* cells. At least two members from a group should be the same word and L can be as large as X. For example, if there are four upsets in a memory at a certain time, the four cell upsets can be mapped to the groups with 2, 3, or 4 member cells. At least two member cells at each group should be at the same word. If the four events land on one cell, the SEC code can fix the error and the case is not considered in calculating the failing probability. G_L can be expressed as "(6)."

$$G_L = \binom{M}{L} - \binom{W_{ID}}{L} \cdot B_{ID}^{\ L} \quad (6)$$
$$= \binom{W_{ID} \cdot B_{ID}}{L} - \binom{W_{ID}}{L} \cdot B_{ID}^{\ L}$$

The second term in the right hand side of (6) shows the number of groupings where all members belong to different word locations with interleaving distance (ID) considered.

When *X* upsets are mapped to G_L groups, the upsets can be assigned to the cells in each group in different sequences. ${}_L T_X$ represents all such cases when *X* upsets are assigned to each group. In the assignments, each upset, including those in an MCU, is assumed to be produced one at a time in probabilistic calculations. For example, an event can create multiple upsets, which are assumed to be created sequentially and mapped to the cells in each group with L members. Since the MCU is already accounted for in the CP model, such mapping would not negatively impact the probability analysis. ${}_L T_X$ can be expressed as in "(7)". Please note that multiple upsets of *X* can be assigned to a cell location, but all cells in the *L* locations should be fully used in the mapping. Every time an event is mapped to a cell location, the mapping probability is *1/M*, as shown in the last term in "(5)".

$${}_L T_X = {}_L \Pi_X - \left[\binom{L}{L-1} \cdot {}_{L-1} T_X + \binom{L}{L-2} \cdot {}_{L-2} T_X + \cdots + \binom{L}{1} \cdot {}_1 T_X\right] \quad (7)$$
$${}_1 T_X = {}_1 \Pi_X$$

This analytical model is quite complex and has not been validated. Therefore the first objective of this paper is to check by simulation that the model is correct.

In the derivation of the model, all upsets were treated like an SEU to calculate the failure probability in "(5)." Therefore all upsets were assumed to have equal probability of landing on any memory cell. However, when there are X upsets in a memory, there is a probability that some of them are clustered in MCU cases, in which case, equal probability cannot be applied.

When multiple upsets are clustered, the number of failing cell combinations, G_L, is less then when errors are independent as certain groupings are not feasible because of the clustered upsets. Such impossible groups cannot be considered as a failing. As a result, the failing probability without consideration of error grouping in MCUs, $P_{f:SEU}$, is greater than the failing probability with MCU consideration, $P_{f:MCU}$, as shown in "(8)."

$$P_{f:MCU}(X) < P_{f:SEU}(X) \quad (8)$$

Supposing that the interleaving distance (ID) is large enough that an MCU cannot or negligibly affect a failure across an interleaving window, the failure model in "(5)" can provide an upper bound on the failure probability by treating the MCU event like multiple SEU events. Estimating how close this upper-bound is to the real $P_{f:MCU}$ is the second objective of this paper which is also done by simulation.

III. Model Validation

To validate the proposed analytical model the implementation of the model reported in [7] has been compared with simulations. The simulations assume Poisson arrivals for the error events and a geometric distribution of the number of errors per event. Additionally the errors within an event are assumed to be independent that is for each error a cell is randomly selected among all memory cells. These are the assumptions used in the derivation of the analytical model reviewed in Section II. The simulations reproduce in a probabilistic way the errors that would occur in the memory after a given radiation time and then the errors are analyzed to

see if they would cause a failure. The process is repeated 100 million times to get an accurate estimate of the failure probability. A constant memory size of M =16Kbits is used with different word sizes B ranging from 64 to 4 so that the number of words W ranges from 256 to 4096. These are the same configurations that were used in [7] to analyze the model. The results for r = 0.2 are shown in Fig. 1 where the model results are plotted with circles and the simulation results with asterisks for different ID values. The results are in good agreement with the simulations. The ratio of the simulation results and the one computed using the model for values of r from 0.1 to 0.9 are illustrated in Fig. 2. Again the model calculations match the simulation results except for some deviations when the failing probability is very small. This is due to the fact that the accuracy of the simulations is not very good for very low failure probabilities.

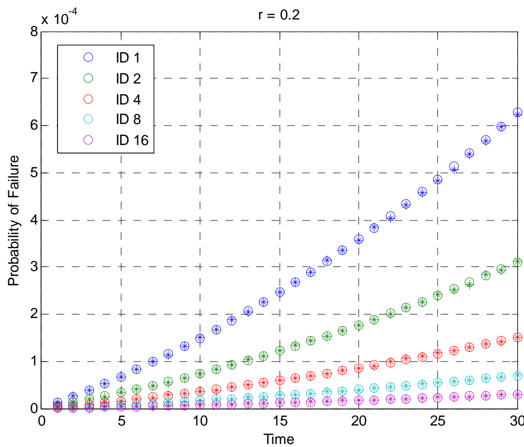

Fig. 1. Failing probability with λ=0.01, r= 0.2, and X=1-30 for model and simulation.

Additional simulations including all the cases reported in the following section have been done to check the accuracy of the model for larger radiation times and different memory sizes. In all cases the model and simulation results are in good agreement.

IV. ACCURACY OF THE MODEL

In the previous section the model has been validated by simulations based on the same assumptions used to derive the model. The model assumes that the errors within an MCU are independent that means that two errors of the same MCU can occur on the same word. This is conservative as in a real memory when sufficient interleaving distance is used, the errors of an MCU will always occur on different words. In this section we evaluate the accuracy of the model by running simulations in which the errors with-in an MCU are forced to occur in different words. These simulations should be closer to the real failure probability than that of the analytical model and therefore are used to see how conservative the model is in different situations.

In the first experiment r= 0.5 which is a value that can be used to model the MCUs observed in 65nm and 45nm SRAMs in the experiments reported in [7] is studied. In Fig 3 the ratio of the failure probability predicted by the model and observed in simulation when the errors in an MCU are forced to occur in different words is illustrated. It can be observed that the relative error introduced by the model assumptions is larger for smaller radiation times. This plot clearly shows a convergence towards a ratio of one when the radiation time is large. This is expected as for longer radiation times there are more error events and the probability of failure among errors of different events becomes much larger than that of failure by errors in the same event.

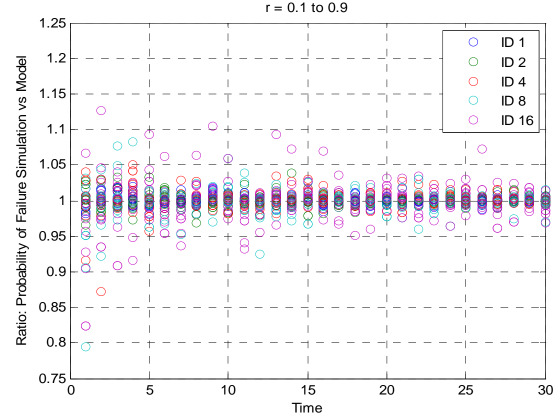

Fig. 2. Ratio of failing probability with λ=0.01, r= 0.1-0.9, and X=1-100 for simulation and model.

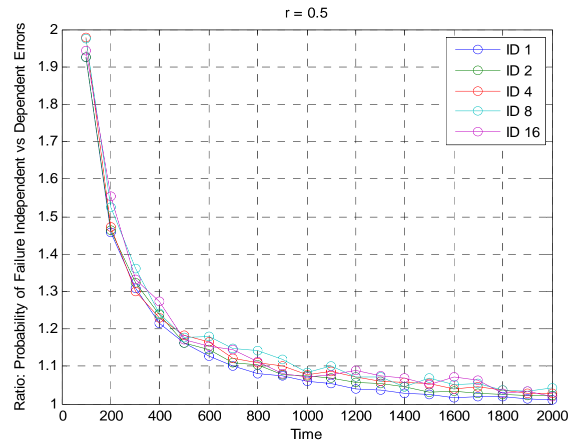

Fig. 3. Ratio of predicted and observed in simulation failure probabilities for r = 0.5.

In Fig 4 the results for r= 0.1 are shown in terms of the failure probabilities ratio. It can be observed that the accuracy of the model is better than in the previous case. This is again expected as for lower values of r there are fewer errors per event and therefore the probability of failure due to errors of the same events are lower.

From those results the main observation is that the model is more accurate for large radiation times and small values of r as expected.

In the previous experiments a memory of constant size varying the word width has been used. It is also interesting to look at memories of different sizes and constant word width to see how accurate the model is with memory size. In Fig 5 those results are presented for memories of different sizes and a word width B of 16 bits. It can be seen that the accuracy of the model is better for larger memories. In that case, the model is accurate for low radiation times and failure probabilities. This is expected as for larger memories more error events are needed to cause failure and therefore the effect of failures due to errors on the same MCU become smaller. At the same time a larger

memory will suffer more particle hits and therefore the event arrival rate will be larger meaning that less radiation time is needed to induce the same number of errors in the device. This is an important result as it means that the model is more accurate for larger memories. This is very convenient as memory size is increasing continuously in real designs.

Additional results for r=0.1 are shown in Fig 6 showing that the model is more accurate for lower values of r as expected.

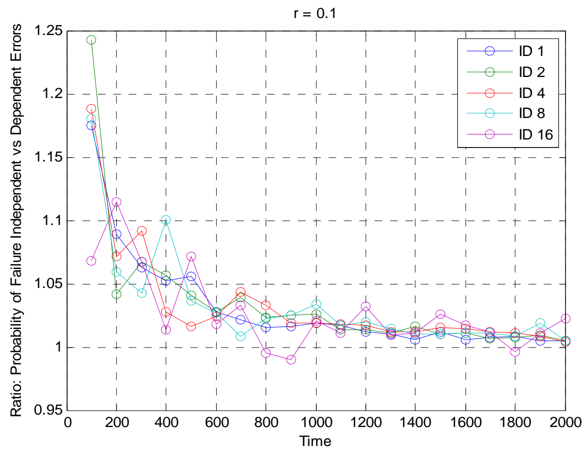

Fig. 4. Ratio of predicted and observed in simulation (with dependent MCU errors) failure probabilities for r = 0.1.

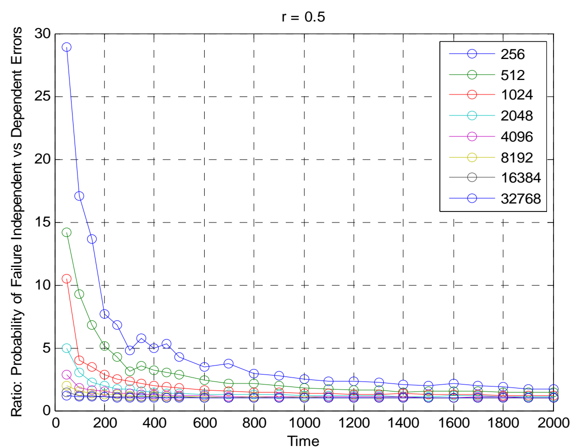

Fig. 5. Ratio of predicted and observed in simulation failure probabilities for r = 0.5 and different memory sizes.

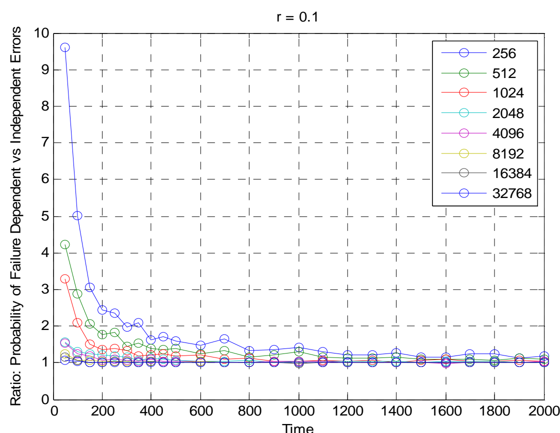

Fig. 6. Ratio of predicted and observed in simulation failure probabilities for r = 0.1 and different memory sizes.

V. Conclusions

MCU are dominant events in technology sizes equal to or smaller than 65 nm and cannot be ignored or treated as negligible in reliability analysis. In this paper a model recently proposed to capture MCU effects has been validated by simulation. As the model does not capture all MCU effects, (in particular it does not account for the clustering effects of MCU errors) the accuracy of the model has also been checked by simulation showing that it can be used to accurately forecast the real failing probability in most situations. The analysis shows that the model is more accurate for larger memory sizes and larger radiation times. These results can facilitate the use of the model in the design process to drive optimum soft-error design decisions.

References

[1] E. Ibe, S. Chung, S. Wen, H. Yamaguchi, Y. Yahagi, H. Kameyama, S. Yamamoto, and T. Akioka, "Spreading Diversity in Multi-cell Neutron-Induced Upsets with Device Scaling," IEEE Custom Integrated Circuit Conference, pp. 437-444, 2006.

[2] Y. Kawakami, M. Hane, H. Nakamura, T. Yamada, and K. Kumagai, "Investigation of Soft Error Rate Including Multi-Bit Upsets in Advanced SRAM Using neutron irradiation test and 3D mixed-mode device simulation," 2004 IEDM, pp.945-948, Dec. 2004.

[3] D. Radaelli, H. Puchner, S. Wong, and S. Daniel, "Investigation of multi-bit upsets in a 150 nm technology SRAM device," IEEE Trans. Nucl. Sci., vol. 52, no. 6, pp 2433-2437, Dec. 2005.

[4] Y. Tosaka, H. Ehara, M. Igeta, T. Uemura, H. Oka, N. Matsuoka, and K. Hatanaka, "Comprehensive study of soft errors in advanced CMOS circuits with 90/130 nm technology," *IEDM*, pp. 941-944, Dec. 2004

[5] P. Reviriego, J. A. Maestro, and C. Cervantes, "Reliability analysis of Memories suffering multiple bit upsets," IEEE Trans. On Device and Materials Reliability, vol. 7, no 4, pp 592-601, Dec. 2007

[6] S. S. Mukherjee, J. Emer, T. Fossum, and S. K. Reinhardt, "Cache Scrubbing in microprocessors: myth or necessity?," 10th *IEEE Pacific Rim International Symposium on Dependable Computing*, pp. 37-42, Mar. 2004.

[7] S. Baeg, S. Wen and R. Wong "SRAM Interleaving Distance Selection with a Soft Error Failure Model" Proc. of European Workshop on Radiation Effects on Components and Systems (RADECS), Jyvaskyla (Finland), Sept 2008, pp 306-310.

[8] M. Sahinoglu, "Compound-Poisson software reliability model," in *IEEE Trans. on Software Engineering*, vol. 18, no. 7, pp 624-630, July 1992.

[9] N. R. Barraza, B. Cernuschi-Frias, F. Cernuschi, "A probabilistic model for grouped events analysis," Proc. IEEE Int'l Conf. Systems, Man Cybernetics, vol. 4, pp.3386-3390, Oct. 1995.

[10] S. Satoh, and Y. Tosaka, "Geometric effect on multiple-bit soft errors induced by cosmic ray neutrons on DRAM's", IEEE Electron Dev. Lett., vol. 21, no. 6, pp310-312, June 2000.