Study of the Effects of Multibit Error Correction Codes on the Reliability of Memories in the Presence of MBUs

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***Abstract*—Failures produced by soft errors in memories because of radiation or similar causes are an important problem due to the large impact that this issue has on the systems where they operate. There are several techniques that offer good results against single event upsets (SEUs), like single error correction–double error detection codes. However, there may be situations where these solutions are not enough, for example, when there is a large SEU arrival rate or multiple bit upsets (MBUs) are present. This last situation is becoming more frequent as technology scales, since in this case, the probability that a single event induces several errors in adjacent cells is higher. A possible solution to address this problem is the use of multibit protection codes, which are often utilized in other fields like communications. However, there are no developed models for memories that can put in perspective how these multibit protection codes behave in the presence of MBUs, and how the reliability of the system is affected by its use. In this paper, a reliability analysis of this case will be presented, studying how the proposed model behaves with respect to the traditional SEU ones and offering some applicability conditions. Both scenarios of memories with and without scrubbing will be analyzed, and several simulation results will be offered in order to prove the accuracy of the proposals.**

***Index Terms*—Memory, multibit error correction codes, multiple bit upsets (MBUs), reliability.**

I. Introduction

Soft errors are an important problem in electronic systems, particularly due to the increasing level of integration of recent circuits. There are many causes that may induce soft errors. This is particularly visible in hostile environments, where there are physical phenomena that affect semiconductors in a negative way. Radiation [1]–[3] is one of these factors, and its influence in errors has been reported many times [4], [5]. Space applications are particularly critical, since systems are not easily accessible, and therefore, errors may produce the complete failure of a mission [6]–[8].

Among the different modules that can be found in digital circuits, memories [9]–[11] are usually the most affected by single event upsets (SEUs) [12]–[15]. Errors in memories usually disturb a single cell, but they may also produce more important problems, as a row/column failure (if the error strikes on the row/column selector) or even a whole chip failure (if the error strikes on the chip selector).

Memories are usually protected by codes that can correct single errors and detect double ones in a given word, what is known as SEC–DED [16]–[19]. This may be achieved by using redundancy, for example, Hamming codes [20], [21]. With this, an extra cost overhead is introduced, which is the one associated to the redundant bits. Moreover, adding extra hardware increases the probabilities of suffering an SEU, since the number of storage elements is also higher.

There are situations in which SEC is not enough. This may be due to a large event arrival rate [22] or the presence of multiple bit upsets (MBUs) [23]. MBUs [24]–[28] are becoming increasingly common for advanced memory technologies and pose a major problem as they make SEC codes ineffective.

To tackle this problem, several approaches may be followed of which one is to use higher order protection codes that can correct more than one error simultaneously. This approach relies on the use of a larger number of redundant bits, what makes the correction process more complex.

Examples of these codes are the Reed Solomon [29], the Golay [22], or even the extension of Hamming codes. The problem with this kind of codes is that the cost needed to implement them is higher, and the processes to codify and decodify data are more complex. How cost and complexity grow depends on the type of code used, but they are always more difficult to handle than SEC codes.

Another approach to deal with multiple errors due to MBUs in memories is interleaving [30]. This technique separates the different bits of a logical word into different physical positions, following a determined pattern. If an MBU hits a memory, it is sure that it will affect adjacent bits, since the effect of the energetic particles is very local to the impact area. However, due to the effect of interleaving, these adjacent bits would belong to different logical words. This means that each logical word would only have an error in one of its bits, which can be corrected by SEC codes. In order to assure this, the interleaving distance (which is the physical distance of the bits that form the same logical word) should guarantee that bits are separated enough out of the effect area of a single MBU [31], [32].

However, there may be certain situations in which interleaving is not feasible. One of these situations is when working with small memories [23]. If the size of the memory is reduced, then it may not be possible to separate enough the bits in the same logical word. Therefore, MBUs would eventually

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produce a failure in the system. Another example of this kind of memories is content addressable memories [23], in which separating the bits of the same logical word may lead to a large layout complexity or even be unfeasible.

There may be other situations in which size is not a problem, but implementation difficulties and cost can prevent the use of interleaving. If any of these scenarios happen, the only possibility is the use of protection codes for more than one bit, as discussed before.

The reliability offered by multibit protection codes has been previously studied [22] in memories that suffer only SEUs. However, to the best of the authors' knowledge, there is no previous work on how these codes behave when both SEUs and MBUs are present. The goal of this paper is to analyze how memory reliability is affected by the use of such codes, studying the mean time to failure (MTTF) of the system as a figure of merit.

This paper is organized as follows. In Section II, the reliability models will be described and compared with the traditional SEC case. In Section III, the models will be contrasted with several simulation experiments. Finally, in Section IV, the conclusions and future work will be presented.

II. Reliability Study of Multibit Correction Codes

When interleaving is not used, MBUs are likely to affect multiple bits of the same word, having a large effect in the reliability and, thus, in the MTTF. In the rest of this paper, codes that can correct L bits will be assumed, where L is equal to the maximum number of errors that an MBU can produce on a given word. With this assumption, isolated MBUs could never produce a failure, since at least two events in the same word would be needed to cause an uncorrectable error. Smaller values of L will result in a significant reduction of the MTTF, as isolated events could cause a memory failure. For larger values of L, the cost would be excessive in most cases due to the extra protection bits and the combinational logic in order to detect and correct errors.

Two studies will be presented next: the first one for memories without scrubbing and the second one for memories in which scrubbing has been implemented.

A. Analysis of the Nonscrubbing Case

1) Initial Analysis—$L = 2$: For the initial analysis, only two-error MBUs and codes that can correct two errors per word will be considered. In this case, the MBUs of interest are the ones that affect 2 bits of the same memory word. If words correspond to rows, then those MBUs would be horizontal. Let us denote the probability of an event causing a horizontal 2-bit MBU by $p2$. Then, a failure in a given word can be caused by three consecutive SEUs, by a combination of a horizontal MBU and an SEU or by two horizontal MBUs. As a first approximation, only the failures caused by combinations that involve at least a horizontal MBU will be considered. In this case, since scrubbing is not used, errors will accumulate in the memory so that the probability of failure will increase for each new event. For a memory with M words and assuming k previous events, the probability of failure upon the reception of event $k+1$ can be approximated by

$$P_f(k+1)\big|_{\mathrm{MBU}}^{M} \cong \frac{p2\cdot(k) + (1-p2)\cdot k\cdot p2}{M} = \frac{k\cdot p2\cdot(2-p2)}{M}. \tag{1}$$

The first term corresponds to the probability of producing a failure due to event $k+1$ (SEU or MBU) occurring on a word previously affected by a two-error MBU. This is given by the average number of words that will have been affected by an MBU in the previous k events $(p2\cdot k)$, divided by the total number of memory words M. The second term is the probability of producing a failure due to event $k+1$ being an MBU and occurring on a word previously affected by an SEU. This is given by the average number of words that will have been affected by an SEU in the k previous events $(1-p2)\cdot k$, divided by the total number of memory words M and multiplied by the probability that event $k+1$ is an MBU $(p2)$.

Approximation (1) gets better for large values of k.

Considering that the same probability for a memory affected only by SEUs with SEC protection is

$$P_f(k+1)\big|_{\mathrm{SEU}}^{M} = \frac{k}{M}. \tag{2}$$

Then, the MBU case with double correction codes can be seen as a memory with SEC protection being affected only by SEUs but with a larger memory size M'

$$P_f(k+1)\big|_{\mathrm{MBU}}^{M} \cong \frac{k\cdot p2\cdot(2-p2)}{M} = \frac{k}{M'} = P_f(k+1)\big|_{\mathrm{SEU}}^{M'} \tag{3}$$

where M' is defined as

$$M' = \frac{M}{p2\cdot(2-p2)}. \tag{4}$$

This implies that using protection codes of 2 bits for MBUs of that size would reduce the probability of failure with respect to the SEC protection for SEUs, what can be virtually seen as having a memory of larger size.

Moreover, the MTTF of a memory protected by SEC codes, suffering SEUs with an arrival rate per memory of λ and a size of M words, can be approximated, for large values of M and assuming Poisson arrivals, by [17]

$$MTTF\big|_{\mathrm{SEU}}^{M} \cong \frac{1}{\lambda}\cdot\sqrt{\frac{\pi\cdot M}{2}}. \tag{5}$$

Again, the MBU case with double protection can be seen as the SEU case with SEC protection but with a memory size M'

$$MTTF\big|_{\mathrm{MBU}}^{M} \cong \frac{1}{\lambda}\cdot\sqrt{\frac{\pi\cdot M}{2\cdot p2\cdot(2-p2)}} = \frac{1}{\lambda}\cdot\sqrt{\frac{\pi\cdot M'}{2}} = MTTF\big|_{\mathrm{SEU}}^{M'}. \tag{6}$$

Instead of modeling the double error protection codes (protecting two-error MBUs) with the SEU case affecting a bigger memory, this can also be seen as the SEU case but with a lower event arrival rate λ'

$$MTTF\big|_{\text{MBU}}^{\lambda} \cong \frac{1}{\lambda} \cdot \sqrt{\frac{\pi \cdot M}{2 \cdot p2 \cdot (2 - p2)}}$$

$$= \frac{1}{\lambda'} \cdot \sqrt{\frac{\pi \cdot M}{2}} = MTTF\big|_{\text{SEU}}^{\lambda'} \qquad (7)$$

$$\lambda' = \lambda \cdot \sqrt{p2 \cdot (2 - p2)}. \qquad (8)$$

In summary, the case of memories suffering two-error MBUs protected with double error correction codes can be approximated with the case of memories protected with SEC codes suffering SEUs but with either a larger size or a lower event arrival rate. This is a convenient approach, since the SEU case is a well-known scenario, which simplifies the process of handling MBUs.

These results cover only the failures in which at least an MBU is involved. Therefore, the approximations would be valid when most of the failures are caused by MBUs. Obviously, that is the case when $p2$ is large.

Let us study some criteria in order to guarantee that MBUs are the dominant failure effect over SEUs.

2) Conditions for the Approximation Applicability: First, let us consider the probability of failure due to SEUs for a low number of events. Considering the MTTF [see (5)] and the relation for Poisson processes $MTTF = METF/\lambda$, (where METF is the mean number of events to failure [33]), it can be determined that the mean number of SEUs to produce a failure with SEC codes would be $\sqrt{(\pi \cdot M)/2}$ (statistically, these events would produce two errors in the same word).

If, now, double error protection codes are used, an extra error would be needed in the same word. The probability that the $\sqrt{(\pi \cdot M)/2} + 1$ SEU produced a third error happening in the same word would be $1/M$ on average

$$P_f\left(\sqrt{\frac{\pi \cdot M}{2}} + 1\right)\Bigg|_{\text{SEU}} \cong \frac{1}{M}. \qquad (9)$$

On the other hand, the probability of three errors in the same word due to MBUs with $\sqrt{(\pi \cdot M)/2} + 1$ events $(M \gg 1)$ would be given by (1)

$$P_f\left(\sqrt{\frac{\pi \cdot M}{2}} + 1\right)\Bigg|_{\text{MBU}} \cong \sqrt{\frac{\frac{\pi \cdot M}{2}}{M}} \cdot p2 \cdot (2 - p2). \qquad (10)$$

The ratio of both cases would be given by

$$\frac{P_f\left(\sqrt{\frac{\pi \cdot M}{2}} + 1\right)\Big|_{\text{MBU}}}{P_f\left(\sqrt{\frac{\pi \cdot M}{2}} + 1\right)\Big|_{\text{SEU}}} \cong \sqrt{\frac{\pi \cdot M}{2}} \cdot p2 \cdot (2 - p2). \qquad (11)$$

Intuitively, if this ratio is much larger than one, then most failures are caused by MBUs. The condition for that to occur is (considering $p2 \ll 2$)

$$p2 \gg \sqrt{\frac{1}{2 \cdot \pi \cdot M}}. \qquad (12)$$

This condition is met when M is very large and applies when the number of events is lower than $\sqrt{(\pi \cdot M)/2} + 1$.

Next, the analysis of the memory when the number of events is higher than $\sqrt{(\pi \cdot M)/2}$ will be studied.

The average probability of failure if only SEUs are considered will grow due to additional SEUs falling on words that already have an error.

Let us consider how the probability of failure grows between errors $\sqrt{(\pi \cdot M)/2} + 1$ and $2 \cdot \sqrt{(\pi \cdot M)/2}$. Assuming that M is large, then the increment in the probability of failure at event $\sqrt{(\pi \cdot M)/2} + i$ can be approximated as

$$\Delta P_f\left(\sqrt{\frac{\pi \cdot M}{2}} + i\right)\Bigg|_{\text{SEU}} \cong \frac{\sqrt{\frac{\pi \cdot M}{2}} + i - 1}{M^2}. \qquad (13)$$

The increment occurs when the new event falls on any of the $\sqrt{(\pi \cdot M)/2} + i - 1$ words that have already been affected by a previous error. That occurs with probability $(\sqrt{(\pi \cdot M)/2} + i - 1)/M$ and results in an increment of $1/M$.

Therefore, at event $2 \cdot \sqrt{(\pi \cdot M)/2}$, the probability of failure can be approximated as

$$P_f\left(2 \cdot \sqrt{\frac{\pi \cdot M}{2}}\right)\Bigg|_{\text{SEU}} \cong P_f\left(\sqrt{\frac{\pi \cdot M}{2}} + 1\right)\Bigg|_{\text{SEU}} + \sum_{i=2}^{\sqrt{\frac{\pi \cdot M}{2}}} \Delta P_f\left(\sqrt{\frac{\pi \cdot M}{2}} + i\right). \qquad (14)$$

This probability has been calculated by adding the incremental probability of every accumulated event with the probability of $\sqrt{(\pi \cdot M)/2} + 1$ events, which is the initial point of the interval. Developing the second term as an arithmetic series, the following is obtained:

$$P_f\left(2 \cdot \sqrt{\frac{\pi \cdot M}{2}}\right)\Bigg|_{\text{SEU}}$$

$$\cong \frac{1}{M} + \sum_{i=2}^{\sqrt{\frac{\pi \cdot M}{2}}} \frac{\sqrt{\frac{\pi \cdot M}{2}} + i - 1}{M}$$

$$= \frac{1}{M} + \left(\frac{\sqrt{\frac{\pi \cdot M}{2}} + 1}{M^2} + \frac{2 \cdot \sqrt{\frac{\pi \cdot M}{2}} - 1}{M^2}\right) \cdot \frac{\sqrt{\frac{\pi \cdot M}{2}} - 1}{2}$$

$$\cong \frac{1}{M} + \frac{3 \cdot \pi}{4 \cdot M}. \qquad (15)$$

It can be easily generalized that, for successive intervals $[(n-1)\cdot\sqrt{(\pi\cdot M)/2}+1, n\cdot\sqrt{(\pi\cdot M)/2}]$, the probability is given by

$$P_f\left(n\cdot\sqrt{\frac{\pi\cdot M}{2}}\right)\Bigg|_{\mathrm{SEU}} \cong \frac{1}{M}+\frac{(2n-1)\cdot\pi}{4\cdot M}. \quad (16)$$

This means that the growth of the probability function is not constant and increases with the number of events.

On the other hand, the probability for the MBU case, considering $2\cdot\sqrt{(\pi\cdot M)/2}$, can be approximated by [see (1)]

$$P_f\left(2\cdot\sqrt{\frac{\pi\cdot M}{2}}\right)\Bigg|_{\mathrm{MBU}} \cong 2\cdot\sqrt{\frac{\pi}{2\cdot M}}\cdot p2\cdot(2-p2). \quad (17)$$

This implies a constant growth for each interval of $\sqrt{\pi/(2\cdot M)}\cdot p2\cdot(2-p2)$.

The purpose of this paper is to find out when the growth of the probability function for SEUs reaches the growth of the probability for MBUs. Before that point (for a lower number of events), the impact of SEUs is negligible, and therefore, (1) applies for the MTTF calculation in (7). On the other hand, reaching a number of events beyond that point would produce a higher impact due to SEUs, making the mentioned expressions less accurate.

Therefore, considering (16) and (17), the event interval where the growths of both functions coincide is given by

$$\frac{(2n-1)\cdot\pi}{4\cdot M} \cong \sqrt{\frac{\pi}{2\cdot M}}\cdot p2\cdot(2-p2). \quad (18)$$

Since $(2-p2)\approx 2$, then

$$n=\frac{(p2\cdot\sqrt{2\cdot\pi\cdot M})\cdot\frac{4}{\pi}+1}{2}. \quad (19)$$

This means that the number of events that guarantees that (1) and (7) are valid should be smaller than $n\cdot\sqrt{(\pi\cdot M)/2}$. In other words, the mean number of events (METF) should be much lower than the previous expression

$$METF \cong \sqrt{\frac{\pi\cdot M}{2\cdot p2\cdot(2-p2)}} \ll n\cdot\sqrt{\frac{\pi\cdot M}{2}}. \quad (20)$$

Considering that $(2-p2)\approx 2$ and replacing the value of n given by (19), the following condition is obtained:

$$p2 \gg \left(\frac{1}{4}\cdot\sqrt{\frac{\pi}{M}}\right)^{\frac{2}{3}}. \quad (21)$$

If $p2$ meets that condition, (7) is valid to determine the MTTF of memories under MBUs in an approximate way.

As it was explained before, this expression simplifies the study of the memory reliability, since MBUs are modeled through SEUs, just modifying either the memory size or the event arrival rate.

To finish this section, it is interesting to think about the scenario where failures caused by SEUs are dominant, which is exactly the opposite case to the presented one. In this situation, multibit protection codes would not be used to deal with MBUs but to increase the MTTF of a memory suffering a high SEU rate. In this case, an approximation considering a scenario with only SEUs could be used. This scenario is out of the scope of this paper, and therefore, it will not be further considered.

3) Generalization for Higher Order Protection Codes: In this section, the general case where a code can correct up to L bits per word and MBUs can cause up to L errors in the same word will be discussed. The probabilities that a certain event produces $1, 2, \ldots, L$ errors in a word are given by the set $p1, p2, \ldots, pL$. Moreover, as it was assumed before, the errors caused by only two events on the same word dominate, and therefore, approximation (5) can be used with a modified arrival rate λ'.

The interpretation of this scenario is similar to the previous cases: If the error correction codes protect more than a single error, the reliability of the memory is increased, what can be perceived as a lower arrival rate.

Now, if events may induce up to L errors, the probability that two events in the same word produce a failure is given by

$$P_f|_{\mathrm{two\_events}} = \sum_{i+j>L} p_i\cdot p_j. \quad (22)$$

This is the combination of every pair of events whose combined number of errors adds at least $L+1$, thus exceeding the protection and causing a failure when they occur on the same word. Compare this expression with (1), where the number of combinations for two events to produce a failure is much lower. In this way

$$P_f(k+1)|_{\mathrm{MBU}} \cong \frac{k\cdot\sum_{i+j>L} p_i\cdot p_j}{M}. \quad (23)$$

Replacing this expression in (7), a perceived event arrival rate λ' is obtained

$$\lambda' = \lambda\cdot\sqrt{\sum_{i+j>L} p_i\cdot p_j}. \quad (24)$$

Let us define α as

$$\alpha = \sum_{i+j>L} p_i\cdot p_j. \quad (25)$$

Expressions (13)–(16) may be also used in this case. The purpose is, again, to derive a condition where the probability of failure for two events is much higher than the probability of failure for three events.

Expression (9) applies if we approximate the probability of failure due to three events in the same word to one, which is a conservative approximation.

In this way, (17), which is the probability of failure for $2\cdot\sqrt{(\pi\cdot M)/2}$ events, would be rewritten as (based on α)

$$P_f\left(2\cdot\sqrt{\frac{\pi\cdot M}{2}}\right)\Bigg|_{\mathrm{MBU}} \cong 2\cdot\sqrt{\frac{\pi}{2\cdot M}}\cdot\alpha \quad (26)$$

which implies a constant growth for each interval of $\sqrt{\pi/(2\cdot M)}\cdot\alpha$.

In a similar way to (18), if both failure probability growths are equal, the following is obtained:

$$\frac{(2n-1)\cdot\pi}{4\cdot M} \cong \sqrt{\frac{\pi}{2\cdot M}}\cdot\alpha. \tag{27}$$

Therefore, the interval where the probability of failure for three events grows as fast as the probability of failure for two events [similar to (19)] is now determined by

$$n = \sqrt{\frac{2\cdot M}{\pi}}\cdot\alpha + \frac{1}{2}. \tag{28}$$

Then, the maximum number of events that would guarantee that (6) and (7) are valid expressions is $n \cdot \sqrt{(\pi\cdot M)/2}$. This is achieved through (28), which would lead to the following condition:

$$\alpha \gg \left(\sqrt{\frac{\pi}{2\cdot M}}\right)^{\frac{2}{3}}. \tag{29}$$

If this condition is met, (7) can be used, regardless of the value of L.

Analogously, the equivalent of (12) would be determined by

$$\alpha \gg \sqrt{\frac{2}{\pi\cdot M}}. \tag{30}$$

B. Analysis of the Scrubbing Case

1) Initial Analysis—$L = 2$: In this section, the case in which the memory has scrubbing will be analyzed. It is assumed that the events arrive in the memory, following a Poisson distribution, as discussed before. In this way, the probability that a given number of events i arrive in a certain word during a scrubbing interval t_s for a Poisson process with arrival rate λ per memory and a size of M words (assuming that the arrivals are uniformly distributed) is given by [33]

$$P_a(i) = \frac{\left(\frac{\lambda}{M}\cdot t_s\right)^i}{i!}\cdot e^{-\frac{\lambda}{M}\cdot t_s}. \tag{31}$$

When using SEC codes, a common assumption is that most of the failures are caused by two events on a particular given word. In that case, the MTTF can be approximated by [17]

$$MTTF\Big|_{\text{SEU}}^{\lambda} \cong t_s\cdot\frac{2\cdot M}{(\lambda\cdot t_s)^2}. \tag{32}$$

This approximation is valid when

$$\frac{(\lambda\cdot t_s)^2}{2\cdot M} \ll 1. \tag{33}$$

For the initial analysis, as it was done for the nonscrubbing case, MBUs of only two errors both falling on the same word and a memory protected with a double error correction code will be considered. In that case, the following combinations of two events can cause a failure: two MBUs affecting the same word or an MBU and an SEU affecting the same word. Then, from (31), the probability that a given word fails because of two events is given by

$$\begin{aligned} P_f\Big|_{\substack{\text{two}\\ \text{events}}}\cdot P_a(2) &= \frac{\left(\frac{\lambda}{M}\cdot t_s\right)^2}{2!}\cdot e^{-\frac{\lambda}{M}\cdot t_s} \\ &\quad \cdot (p2\cdot p2 + (1-p2)\cdot p2 + p2\cdot(1-p2)) \\ &= \frac{\left(\frac{\lambda}{M}\cdot t_s\right)^2}{2!}\cdot e^{-\frac{\lambda}{M}\cdot t_s}\cdot(p2\cdot(2-p2)). \end{aligned} \tag{34}$$

Moreover, for three events, as all combinations will cause a failure, the probability is given by

$$P_f\Big|_{\substack{\text{three}\\ \text{events}}}\cdot P_a(3) = \frac{\left(\frac{\lambda}{M}\cdot t_s\right)^3}{3!}\cdot e^{-\frac{\lambda}{M}\cdot t_s}. \tag{35}$$

Failures caused by MBUs will be dominant when

$$P_f\Big|_{\substack{\text{two}\\ \text{events}}}\cdot P_a(2) \gg P_f\Big|_{\substack{\text{three}\\ \text{events}}}\cdot P_a(3) \tag{36}$$

which gives

$$p2 \gg \frac{\lambda\cdot t_s}{6\cdot M}. \tag{37}$$

If (37) is met, the majority of failures will be caused by two events, and expression (32) for the MTTF, which corresponds to the SEU case protected with SEC codes, is applicable in this situation. This simplifies the study, in the same way that happened with the nonscrubbing case, and therefore, no extra considerations have to be done because of the MBUs or the higher level protection codes.

The only difference is that the perceived arrival rate is lower than the real one and it would be the same as in the nonscrubbing scenario. As a summary, and considering that the MTTF expression for the scrubbing case is given by (32), the following is obtained:

$$\begin{aligned} MTTF\Big|_{\text{MBU}}^{\lambda} &\cong t_s\cdot\frac{2\cdot M}{(\lambda\cdot t_s)^2\cdot p2\cdot(2-p2)} \\ &= t_s\cdot\frac{2\cdot M}{(\lambda'\cdot t_s)^2} = MTTF\Big|_{\text{SEU}}^{\lambda'}. \end{aligned} \tag{38}$$

As it was mentioned in the nonscrubbing case, the scenario where SEUs are dominant can be studied. This would happen when

$$p2 \ll \frac{\lambda\cdot t_s}{6\cdot M} \tag{39}$$

which is, in fact, the opposite of condition (37).

In this case, the MTTF can be approximated by a model of failure due to three events, e.g., the one used in [22]

$$MTTF\Big|_{\text{SEU}}^{\lambda} \cong t_s\cdot\frac{3!\cdot M^2}{(\lambda\cdot t_s)^3}. \tag{40}$$

2) Generalization for Higher Order Protection Codes: Next, the generalization for L-error protected memories will be discussed. The scenario is very similar to the nonscrubbing case. Let us assume that MBUs can cause up to L errors in the same word with probabilities $p1, p2, \ldots, pL$ and that failures caused by two events will dominate. In this case, approximation (32) can be used with a modified arrival rate λ', being defined by (24).

The probability of failure for two events is also given by (22), and it can also be assumed a probability of failure of one for three events. However, in this case, it is necessary to guarantee that all the events happen in the same scrubbing period (otherwise, they would be corrected). This is achieved by weighing the probabilities with the Poisson expression in (31).

In this way

$$P_f|_{\substack{\text{two}\\\text{events}}} \cdot P_a(2) \gg P_f|_{\substack{\text{three}\\\text{events}}} \cdot P_a(3)$$

$$P_f|_{\substack{\text{two}\\\text{events}}} \cdot \frac{\left(\frac{\lambda}{M} \cdot t_s\right)^2}{2} \cdot e^{-\frac{\lambda}{M} \cdot t_s} \gg P_f|_{\substack{\text{three}\\\text{events}}} \cdot \frac{\left(\frac{\lambda}{M} \cdot t_s\right)^3}{3 \cdot 2} \cdot e^{-\frac{\lambda}{M} \cdot t_s}. \tag{41}$$

Since the probability of failure given three events can be upper bounded by one, the previous expression can be rewritten as

$$P_f|_{\substack{\text{two}\\\text{events}}} \gg \frac{\lambda \cdot t_s}{3 \cdot M}. \tag{42}$$

This is achieved with a low λ (event arrival rate per memory) and particularly with a low scrubbing period t_s. Obviously, the shorter this period is, the less probable the errors can accumulate.

With this probability, the MTTF can be modeled as in the SEU case, with a lower λ

$$MTTF|^{\lambda}_{\text{MBU}} \cong \frac{2 \cdot M}{(\lambda \cdot t_s)^2 \cdot \alpha} = \frac{2 \cdot M}{(\lambda' \cdot t_s)^2} = MTTF|^{\lambda'}_{\text{SEU}}. \tag{43}$$

For the case in which SEUs are dominant, the generalization for L-error protected memories is not as straightforward since different combinations of various MBU sizes can cause a failure with three, four, etc., up to L events. Each of these combinations should be negligible compared to the failures caused by $L+1$ SEUs, in order for these to dominate. The procedure to determine if SEUs are the dominant effect would be the following. First, calculate the probability of failure for i events $1 \leq i \leq L+1$ using the following:

$$P_f|_{\substack{i\\\text{events}}} \cdot P_a(i) = P_f|_{\substack{i\\\text{events}}} \cdot \frac{\left(\frac{\lambda}{M} \cdot t_s\right)^i}{i!} \cdot e^{-\frac{\lambda}{M} \cdot t_s}. \tag{44}$$

If the probability for $L+1$ events is much higher than the rest, then SEUs are dominant, and an approximation for a scenario where only SEUs are present can be used to calculate the MTTF. For example, a variation of (40) could be utilized

$$MTTF|^{\lambda}_{\text{SEU}} \cong t_s \cdot \frac{(L+1)! \cdot M^L}{(\lambda \cdot t_s)^{L+1}}. \tag{45}$$

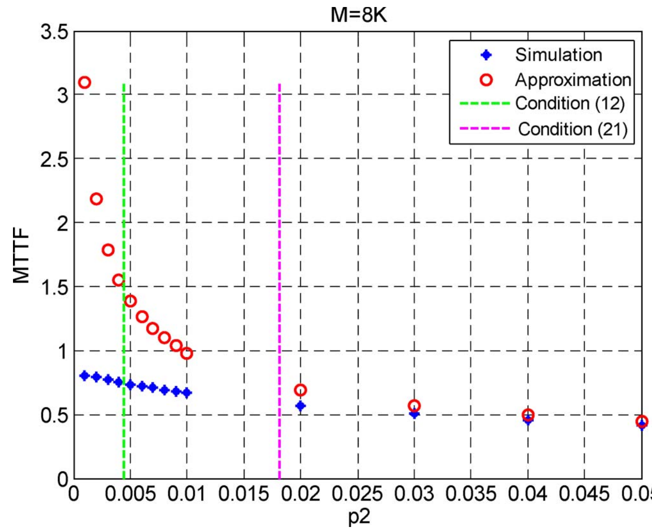

Fig. 1. MTTF versus $p2$ for an 8-Kword memory (nonscrubbing).

III. Simulation Results

In this section, some simulation experiments will be presented, which verify the quality of the models discussed in this paper.

First, the nonscrubbing case will be assessed, and the MTTF derived in (7) will be compared with the one obtained by simulation.

The simulation has been performed on several memories with size $M = 1$ K, 8 K, 64 K, 512 K, 4 M, and 32 Mwords. The event arrival rate per word is 0.1.

The purpose of this simulation is to study the behavior of different memories when exposed to several radiation sources, each one with an increasing proportion of two-error MBUs.

Reaching the threshold defined by (12) and particularly by (21) would indicate a number of MBUs large enough in order for the model to offer consistent results. On the other hand, a lower number of MBUs would imply a high presence of SEUs and, therefore, of failures due to three events, which would deviate from the predicted results.

In Fig. 1, the results obtained for the memory of 8 Kwords are depicted. It can be seen that, as the proportion of MBUs induced by radiation ($p2$) increases, the predicted MTTF using (7) gets closer to the real value obtained through simulation. Once the condition (21) is reached, both values practically coincide.

For the rest of the memories, the ratio of real MTTF/predicted MTTF will be depicted versus $p2$. Obviously, this ratio has to tend to one for the model to work. These results can be seen in Fig. 2.

The first conclusion is that, as the percentage of two-error MBUs grows, the MTTF ratio effectively tends to one.

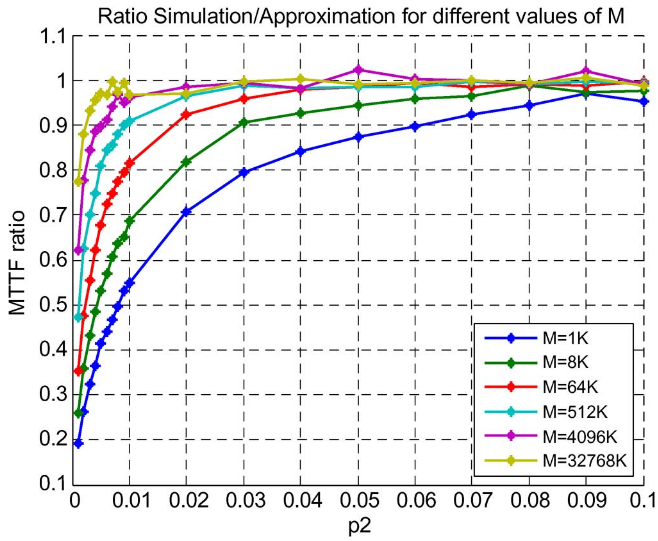

Fig. 2. Real MTTF/predicted MTTF (nonscrubbing).

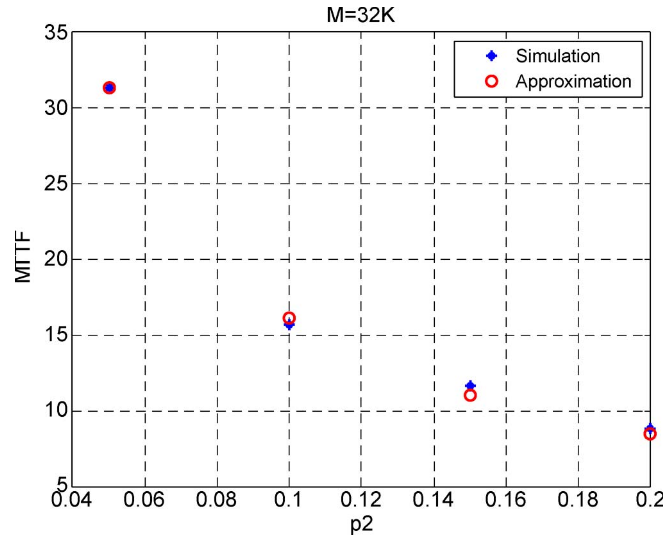

Fig. 3. MTTF versus $p2$ for a 32-Kword memory with scrubbing when approximation (38) is valid.

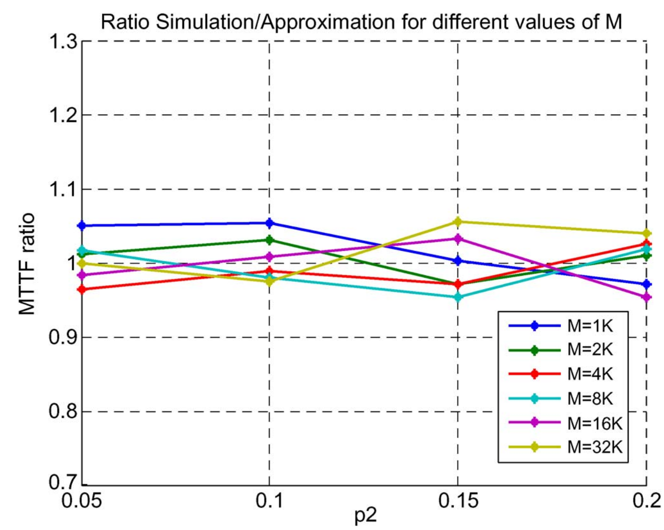

Fig. 4. Real MTTF/predicted MTTF for scrubbing when approximation (38) is valid.

Conditions (12) and (21) are not depicted, since they depend on the memory size. However, a second conclusion that can be reached is that the lower is the M, the higher the $p2$ needs to be in order to get valid results from the approximation. On the other hand, memories with larger sizes reach an MTTF ratio of one more quickly.

In all the cases, the MTTF has been predicted with the expression valid for memories protected with SEC codes against SEUs, with a modified event arrival rate. This proves that, using this simple approach, the case of memories protected with double error correction codes suffering MBUs can be easily modeled.

Next, some simulation experiments for the scrubbing case will be discussed. In this case, memories with size $M = 1$ K, 2 K, 4 K, 8 K, 16 K, and 32 Kwords are used with an event arrival rate per word of 0.1 and different percentages of MBUs ($p2$) ranging from 0.05 to 0.2.

In this experiment, MBU failures are dominant, as

$$p2 \gg \frac{\lambda \cdot t_s}{6 \cdot M} \rightarrow 0.05 \gg 0.0000333.$$

As it was explained before, one condition that has to be met for the model to work is $((\lambda' \cdot t_s)^2/2 \cdot M) \ll 1$. If this is true, the failures produced by two errors are the dominant effect in the model. That is the case of the first experiment, where the scrubbing period t_s is 0.002, so that the largest value for $(\lambda' \cdot t_s)^2/(2 \cdot M)$ is 0.000026.

In Fig. 3, the predicted MTTF is compared with the real one for a 32-Kword memory, for different probabilities of two-error MBUs. It can be seen that both values are very similar, which implies the accuracy of the model.

In Fig. 4, the ratio of real MTTF/predicted MTTF versus $p2$ is depicted for different memory sizes. It can be observed that this value is close to one in all cases, as expected.

Now, the same experiments will be performed but, this time, for $((\lambda' \cdot t_s)^2/(2 \cdot M)) > 1$. This is achieved by setting the scrubbing period to 0.2, so that the largest value of $(\lambda' \cdot t_s)^2/(2 \cdot M)$ is 2.62.

In this second experiment, MBU failures are still dominant as

$$p2 \gg \frac{\lambda \cdot t_s}{6 \cdot M} \rightarrow 0.05 \gg 0.00333.$$

In Fig. 5, the results for the 32-Kword memory are depicted. The conclusion is that the predicted value using the model and the real MTTF are not so close as before, and therefore, the approximation is less accurate, as expected.

In Fig. 6, the ratio of real MTTF/predicted MTTF versus $p2$ is offered. This time, the ratio does not tend to one, which makes the predicted values divergent with respect to the real one. This is more noticeable for larger sizes of the memory. The reason for this is that the event arrival rate λ per memory increases with the size, which makes the $(\lambda' \cdot t_s)^2/(2 \cdot M)$ factor even higher. The same reasoning applies for larger values of $p2$.

Finally, an additional set of experiments has been conducted for the case in which the failures caused by SEUs are dominant,

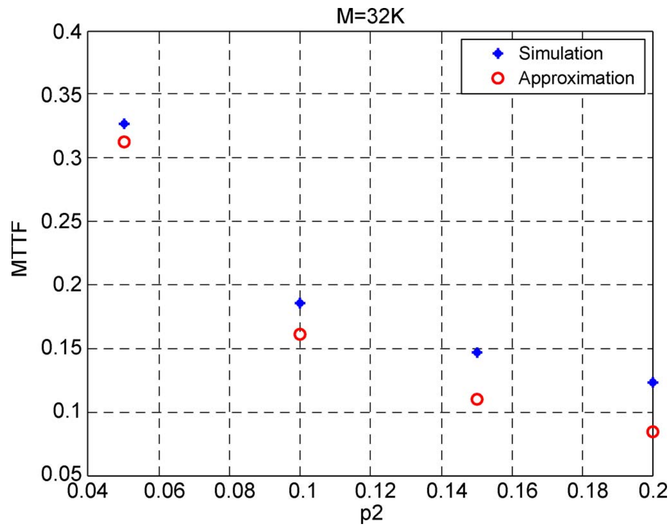

Fig. 5. MTTF versus $p2$ for a 32-Kword memory with scrubbing when approximation (38) is not valid.

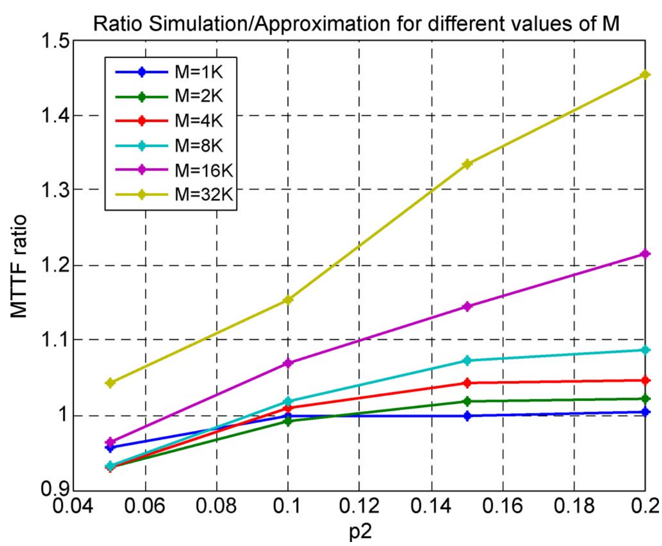

Fig. 6. Real MTTF/predicted MTTF for scrubbing when approximation (38) is not valid.

in order to see if approximations for scenarios where only SEUs are present can be applied with a high precision level.

In this case, memories with size $M = 1$ K, 2 K, 4 K, 8 K, 16 K, and 32 Kwords are also used with an event arrival rate per word of 0.1 and different percentages of MBUs $(p2)$ ranging from 0.00001 to 0.01. The scrubbing period is 0.05. Under these conditions, the values of $p2$ for which failures caused by SEUs are dominant are given by

$$p2 \ll \frac{\lambda \cdot t_s}{3} = 0.00083. \tag{46}$$

In Fig. 7, the results for a 32-Kword memory are presented. It can be observed that, when $p2 \ll 0.00083$, the SEU approximation (45) works well, as SEU failures are dominant as predicted. In Fig. 8, the ratio of real MTTF/predicted MTTF versus $p2$ is offered. The main conclusion is that, when $p2$ meets (46) $(p2 \ll 0.00083)$, the ratios are close to one for all memory sizes as expected.

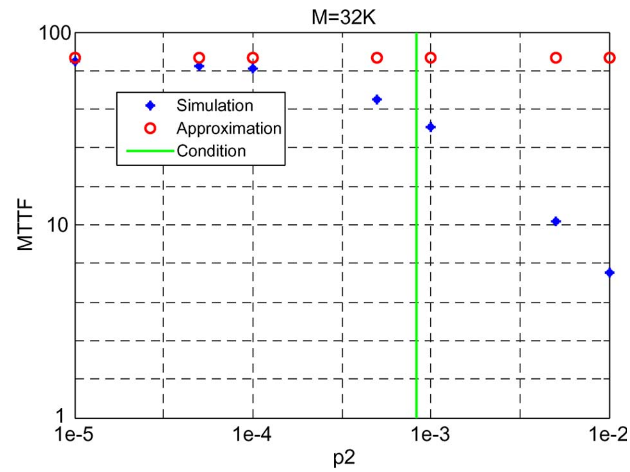

Fig. 7. MTTF versus $p2$ for a 32-Kword memory with scrubbing when SEU failures are dominant.

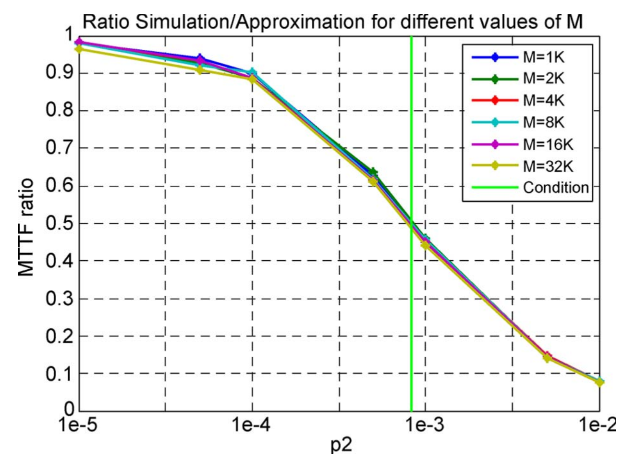

Fig. 8. Real MTTF/predicted MTTF for scrubbing when SEU failures are dominant.

IV. Conclusion and Future Work

In this paper, a model that predicts the reliability (MTTF) of a memory protected with high-order codes under the effect of MBUs has been presented.

The main idea is to use the simpler model of memories protected with SEC codes under SEUs, modifying the perceived event arrival rate, when the effect of MBUs is dominant. In this way, the calculations are highly simplified, making the MTTF derivation easy. Moreover, it has been proved that, when SEUs are the dominant factor over MBUs, a model for SEUs only can be used with a high precision level.

In addition, some conditions have been presented in order to guarantee the applicability of the models. If these conditions are met, the results offered by these models are very similar to the real ones, which has been proved through a wide set of simulations.

About the future work, the first priority will be to corroborate the model with physical experiments, radiating different memories and measuring their reliability. Moreover, the model will be refined in order to consider more failure combinations that are not so dominant, as failures produced by three or more independent events.

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