

Mitigation of permanent faults in adaptive equalizers

P. Reviriego, S. Liu, J.A. Maestro*

Universidad Antonio de Nebrija, C/Pirineos, 55 E-28040 Madrid, Spain

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ABSTRACT

As electronic technology scales, reliability becomes an increasingly important problem. The use of small transistors makes the devices more vulnerable to radiation effects that can lead to permanent failures. Manufacturing defects become also more common due to the small geometries and the large number of transistors used in the integrated circuits (ICs). These defects lower the production yield thus increasing the cost. In this paper those issues are addressed at the system-level for adaptive equalizers that are commonly used in communication ICs. The proposed fault-mitigation approach can be used to deal with both manufacturing defects and permanent failures during the device operation. By exploiting the structure and functionality of equalizers, fault mitigation is provided with negligible area overhead and small performance degradation when a fault occurs.

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1. Introduction

Reliability is becoming a major concern for advanced electronic circuits. As technology scales, smaller devices are used which are more vulnerable to circuit noise and radiation effects. The use of smaller devices and the increase in the number of devices in an IC result also in larger probabilities of having manufacturing defects. These defects, if detected, impact only the production yield increasing the cost. If undetected, they can cause system failures on the field, with potentially large implications. In the coming years, these reliability challenges will increase, as noted in [1]. To address those challenges, a number of alternatives which range from manufacturing to system-level techniques can be used. In this paper, we will focus on system-level techniques.

Failures can be divided in three main categories [2]:

- *Transient*: These failures occur due to temporary environmental conditions like neutron and alpha particles; power supply and interconnect noise; electromagnetic interference and electrostatic discharge. They are summarized as Single Event Effects (SEE) or soft errors.
- *Intermittent*: These occur due to unstable or marginal hardware generated by process variations and manufacturing residuals and can be activated by environmental changes like higher or lower temperature and voltage. They often precede the occurrence of permanent faults.
- *Permanent*: These are irreversible physical changes that occur due to manufacturing defects [3], component aging [4] or sud-

den failures. The two first categories are not a major concern for critical systems as the manufacturing defects are detected during the production testing and component aging is avoided by restricting the useful life of the system.

Some of those failures can be caused, for example, when a circuit is exposed to radiation [5]. Different approaches can be used to deal with failures. One option is to modify the circuit in order to detect failures and to mitigate fault occurrences. In the case of radiation, this can be achieved through the use of special manufacturing processes or radiation tolerant cell structures. Another option is to design the circuit in such a way that when a device fails it does not affect the circuit functionality. This approach is commonly used in memories by incorporating error correction codes that are capable of correcting errors when they occur [6].

For the second approach, generic techniques like Triple Modular Redundancy (TMR) can be used [3]. TMR triplicates the circuit elements and performs majority voting to correct errors. The use of TMR is simple but implies a large cost in terms of circuit area and power. Another alternative is to develop system-level techniques that exploit the circuit functionality to provide fault tolerance [7]. This has been done extensively for signal processing circuits due to their wide use in many applications and to their regular structures that can be exploited to provide efficient protection against failures [8–10].

In particular, adaptive filters have been recently studied to assess the impact of soft errors on some adaptation algorithms [11] and to propose fault-tolerant techniques that exploit the adaptive nature of the filters [12]. Adaptive filters are widely used for equalization in communication circuits [13] and disk storage circuits [14], and in both cases represent a significant part of the circuit area. Therefore, fault mitigation techniques for adaptive equalizers can be useful in many designs.

* Corresponding author. Tel.: +34 914521100; fax: +34 914521110.

E-mail addresses: previrie@nebrija.es (P. Reviriego), sliu@nebrija.es (S. Liu), jmaestro@nebrija.es (J.A. Maestro).

The objective of this paper is to present the proposed fault-mitigation approach for adaptive equalizer implementations that can deal with permanent failures. These implementations would be useful during production to reduce the number of devices that are not usable and once the device is in the field, to increase its operating life in the case that sudden permanent failures occur. The proposed approach is based on dividing the equalizer in two blocks. When a permanent error occurs in one of them that block is disabled and the equalizer continues to operate with only one block. This results in a performance degradation, which is normally small as adaptive equalizers are typically designed to achieve a very low Bit Error Rate (BER) under worst-case channel conditions and operate with a large margin in a typical channel. For instance, some Ethernet transceivers are designed to achieve a BER of 10^{-9} or less for the worst case, which is a cable length of 100 m. However, in real world application, the cables connecting the computers with the switch or router in an office are less than 20 m [15,16]. Therefore, the Signal-to-Noise Ratio (SNR), which is the measurement of the quality of the signal, is overdesigned and this fact is exploited by the proposed technique to implement permanent fault mitigation. In summary the proposed approach uses the over-design of the equalizers when they work in a typical channel to provide fault mitigation. In the case of sudden failures fault mitigation is achieved with a small performance degradation. For manufacturing defects, many defective parts can still be useful as a lower performance version of the original device. This means that the overall number of usable parts is increased.

The rest of the paper is organized as follows. In Section 2, adaptive equalizers are reviewed focusing on a case study. Then, in Section 3, the case study is used to illustrate the proposed approach, which is evaluated in terms of fault mitigation and complexity overhead in equivalent gates in Section 4. Finally, the conclusions of this work are presented in Section 5.

2. Adaptive equalizer case study

In a communication system, signals are sent from transmitters to receivers with the aim of exchanging information. These signals pass through the channel that can be, for example, a cable. The channel introduces distortion on the signals that may cause errors at the receiver. Equalization tries to compensate the effects of the channel on the received signal to minimize errors [17]. Equalization can be done at the transmitter by compensating the channel effects before they occur or at the receiver. In the receiver, one of the typical structures that is used for equalization are Feed Forward Equalizers (FFE). An FFE is an adaptive filter that tries to minimize the observed error in the received signal, as illustrated in Fig. 1. The equalizer is composed of three main elements: a Finite Impulse Response (FIR) filter [18], an adaptation logic block that

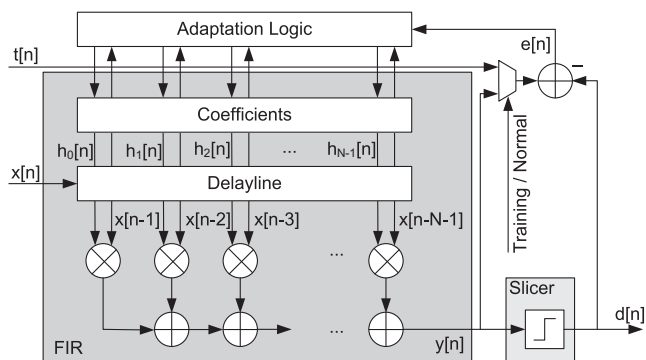


Fig. 1. Block diagram of an adaptive Feed Forward Equalizer.

updates the filter coefficients and a slicer that computes the received symbol.

The Finite Impulse Response (FIR) filter takes the received signal $x[n]$ as an input and filters it to produce and output signal $y[n]$ on which the channel distortion has been compensated. The distortion introduced by the channel will be different for each case. For example, a short cable or a long cable will distort the signal differently. Therefore, the equalization filter should ideally be different in each case. This is achieved with the use of the adaptation logic block that computes the filter coefficients dynamically to adapt to the channel configuration. Finally, the slicer computes the received symbol. This is done by comparing the filter output $y[n]$ with some predetermined thresholds, and choosing the threshold (level) which is closer to $y[n]$ as the slicer output, $d[n]$. The error $e[n]$ is then computed as the difference between $y[n]$ and $d[n]$, or in other words, the distance of the filter output to the closest predetermined threshold.

The adaptation logic tries to reduce the error updating the coefficients $h_i[n]$ as shown in Fig. 2. Basically, the error is multiplied by the delay-line element that corresponds to that coefficient and by a constant alpha, and used to update the coefficient value. The constant alpha controls the adaptation speed and is normally large at start-up to speed up initial convergence and small during steady state. This is so because when the equalizer starts operating it may not have information about the channel and therefore at the beginning equalization will be poor until the filter is adapted. To aid in the adaptation process, in many systems a training sequence $t[n]$ is used at start-up. This is a known sequence of symbols such that the receiver can use it to reliably estimate the error $e[n]$ until the initial adaptation is completed. The typical evolution of $e[n]$ during start-up and steady state is shown in Fig. 3.

To illustrate the proposed techniques, the equalizer shown in Fig. 4 has been used. The filter has 20 coefficients, each coded with 10 bits. The incoming data has eight bits and the accumulators used for adaptation have 30 bits. The adaptation speed is controlled with two values of alpha, 2^{-12} in training state and 2^{-16} in steady state. The channel is low-pass, as is the case in most wire-line communication systems. These parameters are typical values for FFE in Ethernet transceivers [19].

The impulse response used in the simulations is shown in Fig. 5, along with the coefficient values of the equalizer for that particular channel. Finally, two levels are used, -1 and 1 , for the transmitted signal corresponding to one bit per symbol.

The filter coefficients will be different for each channel configuration and the number of coefficients in the equalizer is designed in such a way that it can compensate the channel distortion in the worst-case configuration. This means that in many cases, effective equalization can be achieved with a filter that has fewer coeffi-

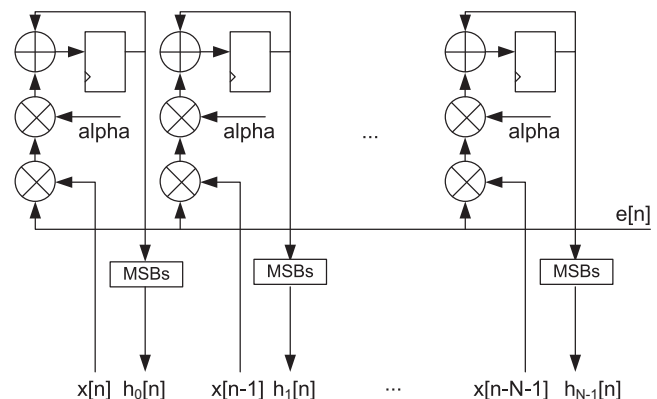


Fig. 2. Block diagram of the Feed Forward Equalizer adaptation logic.

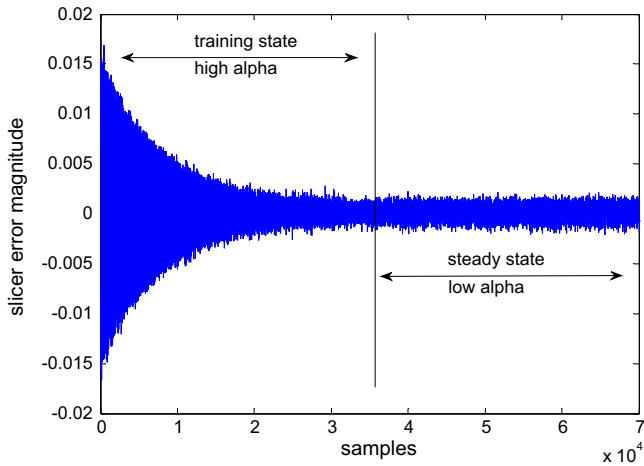


Fig. 3. Slicer error evolution demonstrating the training state and the steady state.

cients. Even for the worst-case configuration, reducing the number of coefficients will only reduce gradually the ability of the equal-

izer to compensate channel distortion. This would increase the number of symbols received in error, but the system may be able to continue operation with a larger bit error rate. This observation about the equalizer performance with a reduced number of taps is used in the following section to propose a protection against permanent failures.

3. Proposed technique

The main idea behind the proposed technique is to decompose the equalizer in blocks, so that when a failure occurs, the block affected is disabled and the equalizer continues operating but with a reduced performance. The failures taken into account are stuck-at failures, where a failure in a device or interconnection causes a signal to stay always at a '0' or a '1'. The proposed technique not only mitigates sudden and catastrophic failures, but also wear-out failures.

The equalizer can be divided in blocks that group some coefficients, as shown in Fig. 6. In this case, two blocks of 10-coefficients are used. The FIR filter can be easily decomposed in two subfilters. The same applies to the adaptation logic where each coefficient operates independently. When the two blocks, FFE_1 and FFE_2,

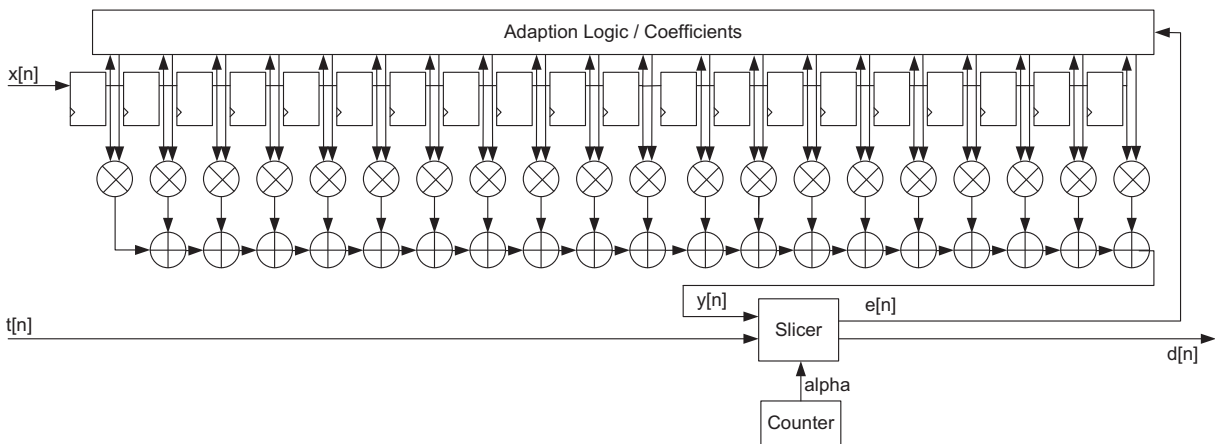


Fig. 4. FFE with 20 tap adaptive filter.

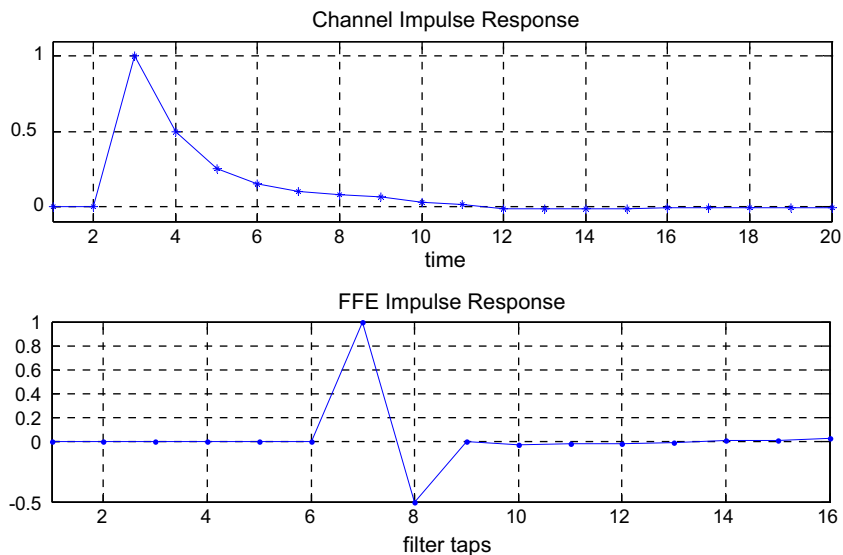


Fig. 5. Channel response used and typical equalizer coefficients after initial adaptation for 20 taps.

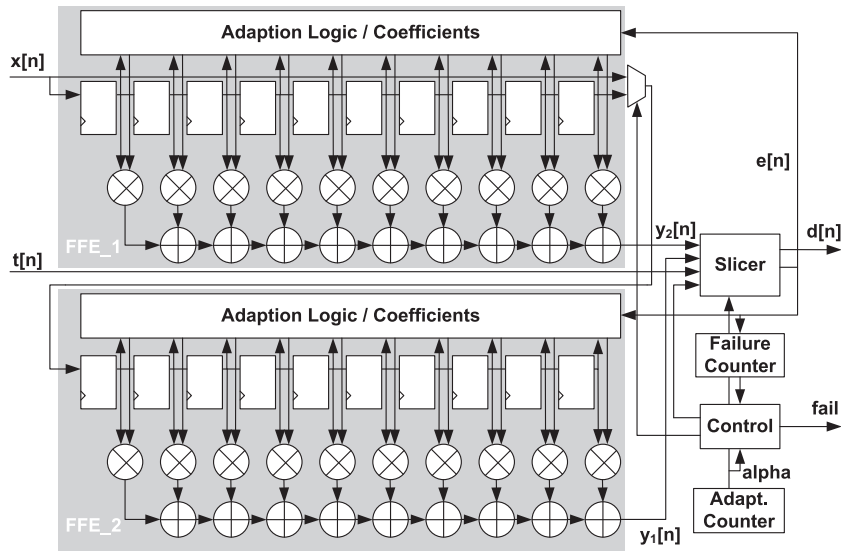


Fig. 6. Block diagram of the Feed Forward Equalizer with permanent fault protection.

are connected in such a way that the output of the delay-line of the first one is the input to the delay-line of the second one, and the outputs of both are added together, the resulting structure is equivalent to that of Fig. 4. That is equivalent to the original equalizer with 20 coefficients except for the switching multiplexer controlling the forwarding of $x[n]$ to the FFE_2, the failure counter and the control unit. Those modules will be described in more detail later when discussing the different work modes of the proposed technique.

This is what is done during normal operation, by adding $y_1[n]$ and $y_2[n]$ in the slicer before the slicing is performed. When a permanent failure is detected, the block affected (FFE_1 or FFE_2) is identified and disabled. In this case the remaining block operates as a 10-coefficient equalizer and enables the system to continue operation. In many cases the performance degradation will be small as the number of coefficients is designed for the worst-case channel and fewer coefficients are needed in the rest of the situations as discussed previously. The different modes of operation are illustrated in Fig. 7, which will be described in more detail in the next sections.

3.1. Normal operation

After the initial phase, the equalizer is working with all coefficients of both blocks in the normal mode, which as discussed before is equivalent to the original equalizer in Fig. 4 (depicted in Fig. 7a). In this situation, the error $e[n]$ should be small and within the limits of the expected error in steady state. Therefore, $e[n]$ can be used to detect if something unexpected is happening. This is illustrated in Fig. 8, where the steady state error is shown along with a failure threshold that in this case has been chosen to be more than double the slicer error level in steady mode. When

the error reaches the failure threshold, that would be an indication that something unexpected might have happened. For example:

- additional noise in the transmission channel,
- a soft error affecting the registers,
- a soft error changing the current value of one of the multipliers or one of the adders,
- or a permanent failure.

Each of these effects may cause a large value in the error. Since we are only interested in permanent failures, the first task is to detect if the unexpected error level is caused by a permanent failure. Once that is done, the equalizer can initiate the error location process and finally reconfigure its mode of operation to disable the block affected by the failure.

3.2. Error classification

The main element to identify that large values of the error $e[n]$ are caused by a permanent failure is their persistence with time. In other words, if the increase in the error level is caused by noise in

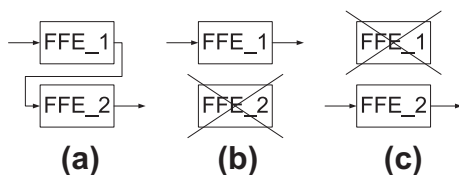


Fig. 7. Working modes of the proposed technique: (a) normal mode, (b) only the first sub-FFE, (c) only the second sub-FFE.

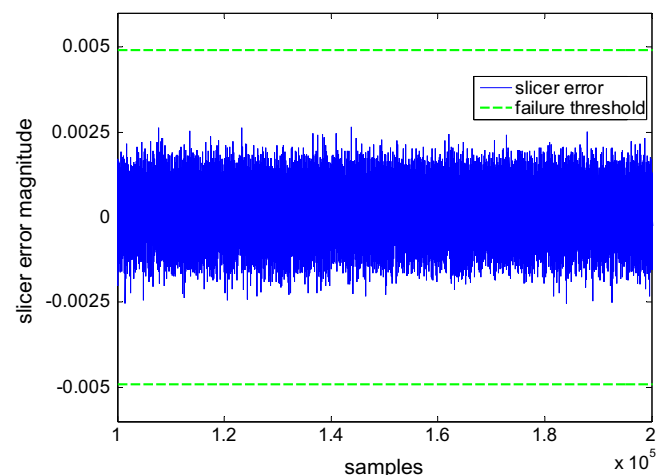


Fig. 8. Slicer error in steady state with the failure threshold marked as a dashed line.

the channel or by soft errors affecting circuit elements, then after some time the error $e[n]$ should return to normal levels. However, if a circuit element has suffered a permanent failure, we would expect to see large values of $e[n]$ indefinitely.

Therefore, permanent fault detection can be performed by checking if the anomalies in $e[n]$ disappear after the maximum duration expected which were measured by soft error injections tests for the other type of errors. Errors caused by noise in the channel have normally a short duration. The same is true for soft errors affecting filter multipliers or adders. Errors in the delay-line registers can last at most N samples. However, errors in the coefficients have an effect on the error that last quite a long time due to the long re-adaption time that can be in the order of thousands of cycles. As an example, the effects of a soft error on the delay-line registers are shown in the top plot of Fig. 9, while the effects of a soft error on the most significant bit of the coefficient registers are illustrated in the bottom plot.

From the previous discussion, permanent errors can be easily identified using the failure counter shown in Fig. 6 that is enabled when $e[n]$ exceeds the failure threshold and increments each cycle. The failure counter is reset and stopped if during a sufficient number of cycles $e[n]$ is below the failure threshold, which is done by a second internal counter. When the failure counter reaches a value that is larger than the number of cycles needed to perform adaptation in the worst case, a permanent failure is detected and consequently the recuperation phase is triggered by the control block (see Fig. 6).

3.3. Recuperation

When the failure counter unit signals the presence of a permanent failure, the control logic starts the first attempt to recuperate the correct functionality by using only the first block and bypassing the second one, as shown in Fig. 7b. In this case, the slicer uses only the filter output $y_1[n]$ of the first block to compute the slicer error calculation, instead of $y_1[n] + y_2[n]$ as done during normal operation. With this configuration, the system performs initial adaptation, and if the error $e[n]$ converges to a level smaller than the failure threshold, the system concludes the recuperation phase. The system will then operate with a reduced number of equalizer coefficients. However, if the error exceeds the threshold for a time

sufficient to trigger permanent failure detection by the failure counter block, then a permanent failure has occurred in the first block. This starts the second attempt of the recuperation sequence. The multiplexer switches the input signal $x[n]$ directly to the second block and the slicer unit considers only the filter output $y_2[n]$ for error calculation, as shown in Fig. 7c. With this configuration, initial adaptation is performed and if the error is smaller than the failure threshold, the system operates only with the second block. Finally, if this second attempt fails, the equalizer sends out a fail signal stating its unrecoverable failure.

A reset of the whole communication system will cause the equalizer to start with the assumption that everything is correct. This gives the equalizer an opportunity to start-up with all of the 20 taps and to check if an intermittent fault that occurred previously is still present. Some faults caused by fluctuation of power supply or the

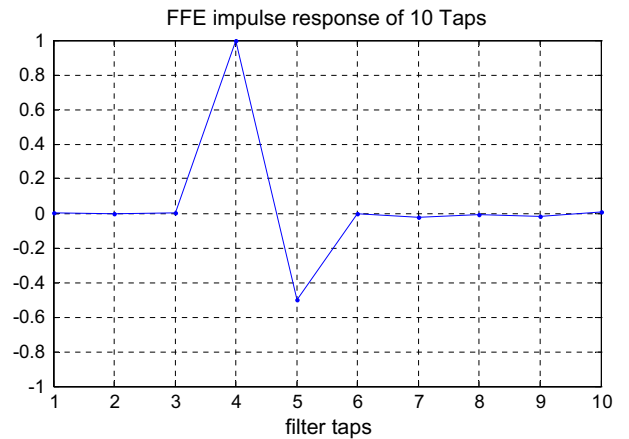


Fig. 10. Equalizer coefficients for 10 taps.

Table 1
Signal-to-Noise Ratio of the FFE with different number of taps.

	20 Taps	10 Taps	Δ SNR
SNR (dB)	27.47	24.92	-2.55

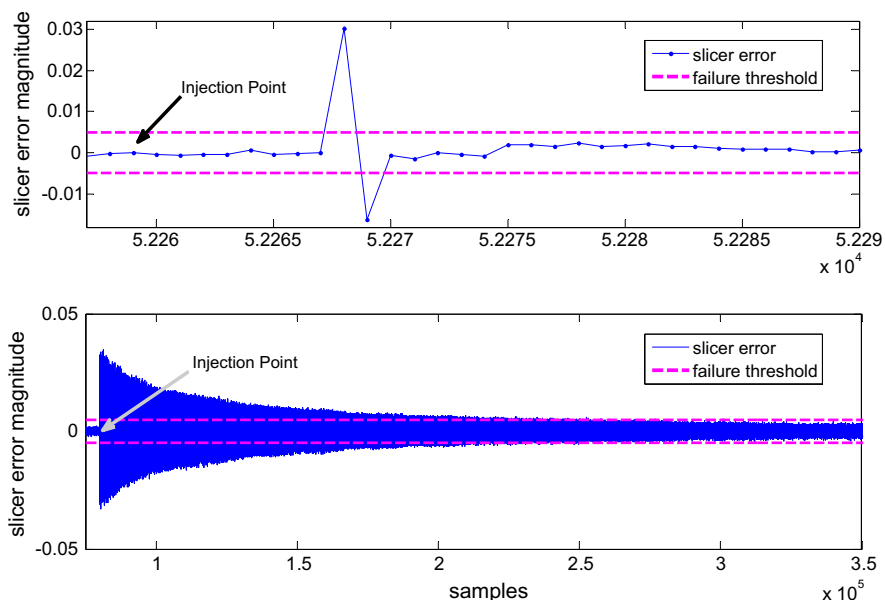


Fig. 9. Impact of a soft error onto the design. The top plot shows the effect on the data delay-line and the bottom one the worst-case effect on the coefficient registers.

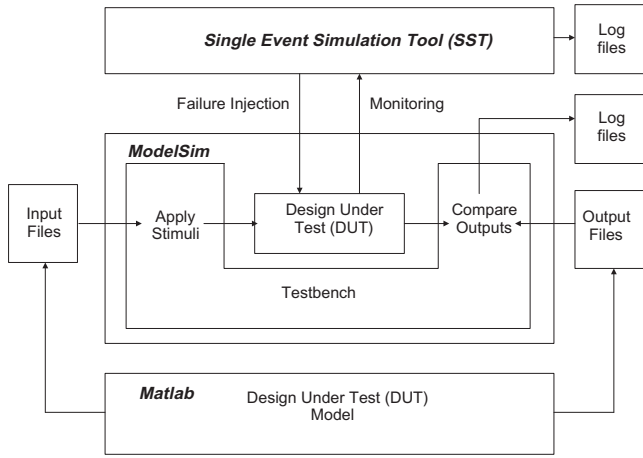


Fig. 11. Simulation environment block diagram.

ground, have a long term transient effect which might disappear after a long time [2]. If that is not the case, the protection mechanism will guarantee that the recuperation process ends up with the correct configuration using one of the equalizer blocks.

The filter coefficients when the equalizer is operating only with one of the blocks are shown in Fig. 10 for the channel response of Fig. 5. It can be observed that the coefficients are similar to the ones used in the original configuration (see also Fig. 5). The overall filter response is similar but does not cover some of the small coefficients at the right side of the original response. This degrades the equalizer performance that in this case translates to a reduction in the Signal-to-Noise Ratio (SNR) from 27.47 dB to 24.92 dB, as shown in Table 1. The SNR gives an indication of the magnitude of $e[n]$ versus the expected signal. The SNR reduction will increase the number of bits received in error but still most of the data frames will be correct and communications can continue with a slightly lower quality. As noted before, the number of coefficients in the equalizer is dimensioned for the worst-case channel, so that

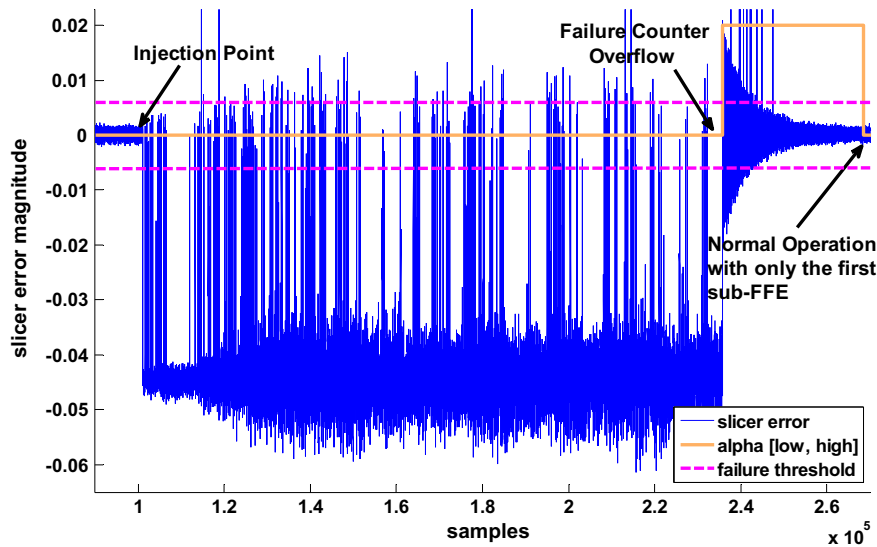


Fig. 12. Evolution of the slicer error in the case of a permanent fault in the second sub-FFE.

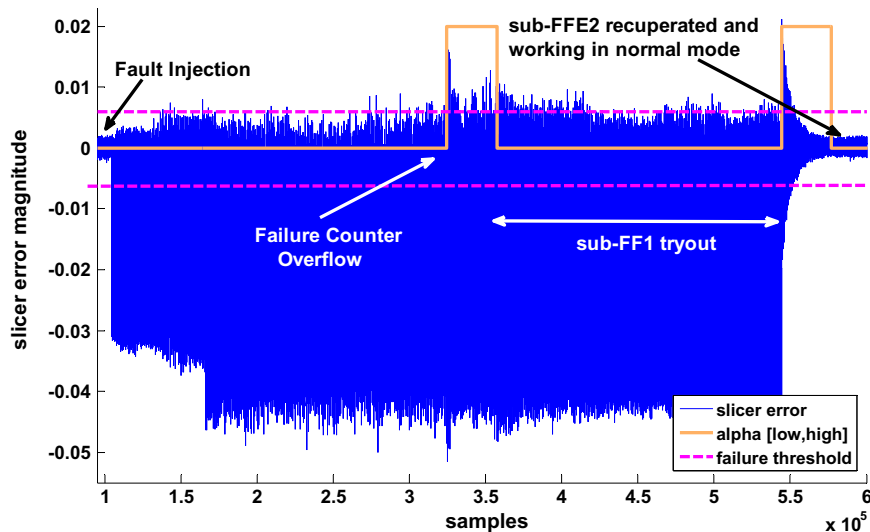


Fig. 13. Evolution of the slicer error in case of a permanent fault in the first sub-FFE.

Table 2
Synthesis results of different FFE implementations using the TSMC 0.35 μm ASIC library.

		Gates	Overhead [%]	Clk [MHz]
Unprotected	SOP + Registers + Adaption logic	38,056	-	34.3
	Slicer	244		
	Adapt. counter	232		
	Total	38,532		
Proposed	FFE_1 and FFE_2	38,056	1.37	34.0
	Slicer	244		
	Adapt. counter	232		
	Switching logic and failure counter and control block	528		
	Total	39,060		
Proposed with partial TMR	FFE_1 and FFE_2	38,056	6.58	33.9
	Slicer	732		
	Adapt. counter	696		
	Switching logic and failure counter and control block	1584		
	Total	41,068		
TMR		115,796	200.52	34.1

in many cases a reduction in the number of coefficients will produce only a minor performance degradation. Therefore, with the proposed technique a permanent fault causes only a small performance reduction.

4. Experimental results

In this section, the effectiveness of the proposed technique is evaluated. To that end, the proposed techniques have been implemented in VHDL and then the circuits have been synthesized for a commercial ASIC library [20]. Then, an experimental setup based on the Single Event Upset Simulation Tool (SST) developed at the European Space Agency [21] has been used to insert errors in the circuit and evaluate their effects showing the effectiveness of the proposed techniques. A block diagram of the experimental setup can be seen in Fig. 11 and a more detailed description can be found in [22]. Naturally, the original tool has been modified so that besides the Single Event Upsets (SEUs) affecting single flip-flops also Single Event Transients (SET) and permanent failures can be injected into the design under test.

For the verification of the proposed protection technique two scenarios where chosen. The first one consists in injecting some

permanent faults into the second block. The second one is doing exactly the same in the first block.

Fig. 12 shows the evolution of the slicer error when a permanent fault is inserted into the second block. The injection was performed during the steady state operation of the equalizer and it causes an abrupt increase in the slicer error $e[n]$, which exceeds the failure threshold (marked in the figure with dashed lines). After the failure counter signals a permanent failure, the control logic recuperation starts by selecting the first block only configuration and performs the initial adaptation, as shown in Fig. 12. Once the training phase ends, the slicer error is within the failure threshold and the equalizer enters the steady state mode of operation.

The second scenario is when the permanent fault occurs in the first block. In this case, the failure counter will signal a permanent failure and the first block only configuration is used. However, as the failure was introduced in the first block, the slicer error exceeds the threshold ending up with a second permanent failure detection. Upon this second failure, the control logic triggers the second recovery attempt, using the second block only configuration. This process is illustrated in Fig. 13, where the failure detections can be seen by the change of alpha from low to high. This second configuration converges to a small error and the equalizer enters the steady state operation.

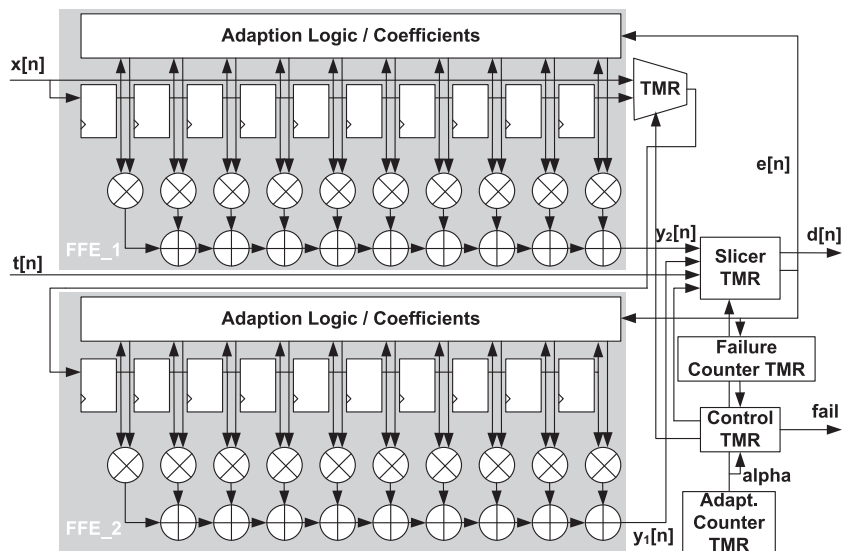


Fig. 14. Block diagram of the Feed Forward Equalizer with permanent fault protection with additional TMR protection.

Finally, in the case of a failure affecting both blocks, the control logic would signal an unrecoverable failure, by sending out the fail signal as indicated in Fig. 6.

In addition to the experiments described, a large number of soft errors have been inserted onto this design to ensure that they are not classified as permanent failures and recuperation is not triggered (two examples are shown in Fig. 9).

The whole design has been synthesized on a commercial ASIC library as mentioned previously and the results of the gate utilization are documented in Table 2. The first thing to note is that the switching logic added to the critical path, has an insignificant impact onto the maximum clock frequency. Another thing to note is that a permanent fault on the control logic can cause an unrecoverable failure, but having a closer look onto the synthesis results shown in Table 2, the slicer unit, adaption counter, failure counter, switching logic and the control logic are very small in comparison to FFE_1 and FFE_2. Therefore, the probability of a permanent fault occurring in one of these blocks is negligible as they only occupy 2.57% of the total area. Additionally, given their small area, those blocks can be protected with TMR as shown in Fig. 14 where the switching logic, the failure and the control logic besides the slicer and the adaptation counter are protected by TMR.

The cost of the equalizer without any protection is compared to the proposed technique protection, the proposed technique with partial TMR and with an ordinary TMR implementation in Table 2. The overall increase of the complexity for the proposed technique is 1.37% and for the proposed technique with partial TMR is 6.58% over the unprotected equalizer. These figures are negligible in comparison with the overhead increase of 200.52% for the straight TMR version. With this increase of 6.58% in complexity, we guarantee that when a permanent failure occurs the system is able to continue operation with a performance degradation that in most cases is small. Therefore, the proposed technique is very effective.

5. Conclusions

An efficient technique has been introduced to protect adaptive equalizers from permanent failures. It has been shown that the study of the protection at the system-level can provide effective fault mitigation techniques. For the adaptive equalizer studied in this paper, dividing the filter in two blocks enables an efficient fault recovery technique by disabling the block in error and operating only with the other block. This ensures that the system continues to operate with a small performance degradation. The cost in terms of area overhead of the proposed technique is very small, 6.6% overhead for the case study considered, which makes it an interesting choice when circuit area or cost is an issue.

The proposed technique could be extended such that n blocks are used instead of two. Then, in case of failure, the number of coef-

ficients would only be reduced by $(n - 1)/n$. Another extension can be to add a redundant block to the equalizer so that when there is a permanent failure the system can still operate with the original performance. For the case study presented this would require an overhead of approximately 50% (three blocks instead of two).

Finally, the same idea could also be applied to other types of adaptive filters, like for example echo cancellers, by dividing the filter into blocks.

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