Validation and Optimization of TMR Protections for Circuits in Radiation Environments

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Abstract— A methodology based on optimization processes and software fault injection is presented to verify and improve TMR protection against SEUs. It allows validating the reliability achieved by the protection, optimizing the solution area cost.

Index Terms— **Single Event Upsets (SEUs), Error Rate (ER), Triple Modular Redundancy (TMR), optimization, fault injection.**

I. INTRODUCTION

Fault tolerance on semiconductor devices has been a meaningful matter since upsets were first experienced in space applications many years ago. Integrated circuits operating in the space environment can be upset by charged particles that generate errors in the system. Therefore, the interest in studying fault-tolerant techniques to keep integrated circuits operational has increased. In order to guarantee circuit reliability against Single Event Upsets (SEU), some mitigation techniques have been proposed in the literature during the last decades [1].

On this respect, this paper presents an automatic methodology, based on optimization and fault injection processes, in order to pursue two main objectives:

- To verify the Single Event Upset (SEU) resilience for circuits that implement TMR. If the hardened circuit does not meet the reliability constraints, the methodology identifies the potential wrong areas in the protection (for example a sensitive register that has not been protected).
- To optimize the area of TMR protections in those cases where the reliability specifications are below 100%. In those cases, implementing full TMR can overprotect the circuit, incurring a too high cost. In this situation, the methodology identifies those nodes that could remain non-tripled, while still meeting the specifications.

In order to test this methodology, a Feed Forward Equalizer [2] has been chosen, as these circuits are widely used in space applications, like communications receivers. In this work, an implementation with full TMR will be tested and optimized by the methodology, assuming a reliability constraint of 99%. This implies an error rate (ER) of 1%.

II. PROPOSED METHODOLOGY

Radiation tolerant circuits need to be checked in order to evaluate if an applied protection technique meets the reliability specifications demanded by the target application. In this paper, a methodology is presented to perform this checking in an automatic way. The proposed methodology, in addition to this checking, goes further and can compute the system optimal area cost for techniques that are implemented in an automatic way, like TMR. The methodology is based on the technique presented in [3], in which circuits are protected against SEUs through a method called Selective TMR, which can be used when the reliability constraint is below 100%. The basic idea of Selective TMR is to triplicate only those registers that are sensitive enough and only those, thus saving area respect to the traditional full TMR approach. Any circuit with this kind of fault tolerant technique can be verified, identifying those weak registers that produce a higher impact on the outputs in the presence of SEUs. So, in this way, the technique not only detects possible defects on the TMR protection, but also identifies those registers that do not need to be tripled (if the reliability constraints are below (100%). The workflow that represents the methodology is described in Figure 1.

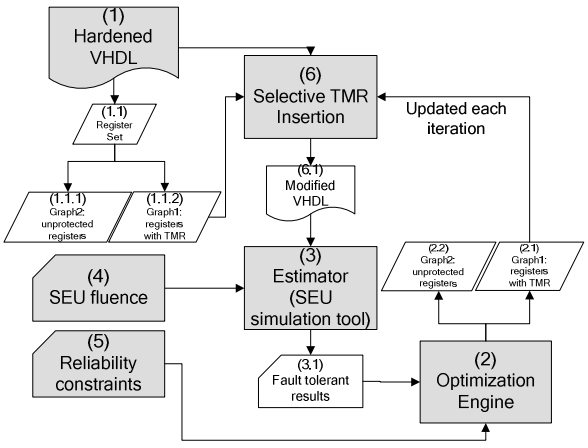

Fig. 1: Methodology workflow

The algorithm is detailed next. First of all, data inputs required by the methodology must include: the target circuit (1), a list of all the registers that are planned to be protected with TMR (1.1.2), the reliability constraint demanded by the application in terms of the tolerated Error Rate (5) and the SEU fluence that the given circuit will supposedly experience (4).

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Next, the checking process is carried out on (1) through an iterative engine (2) based on an optimization algorithm [4], which drives a simulation fault injection routine (3). This methodology measures the Error Rate of the given fault tolerant system in (1.1) through an SEU simulation tool called SST [5] that performs a fault campaign according to (4) (in term of the number of SEUs).
Then, the final circuit with selective TMR is tested with a campaign of injected errors. If the reliability constraint is not met, this means that there are unprotected registers that should have been tripled. In this case, the engine identifies them and applies TMR to them. On the other hand, if the reliability constraint of the final circuit is met, then the methodology goes further and tries to minimize as much area as possible. If the circuit is overprotected and some of the registers do not need to be tripled in order to meet the reliability constraints, then those registers are left unprotected.
In any case, the outputs of the process are two set of registers: protected registers (2.1) and unprotected registers (2.2).

III. CASE STUDY

As mentioned in the introduction, a case study is going to be used to discuss the proposed technique and also to evaluate its effectiveness in a realistic design. The selected filter in this case study is a Feed Forward Equalizer (FFE) [2]. The basic structure is shown in Figure 2, and the proposed methodology has been applied to this FFE implementation in order to test its TMR protection applied over the H_i coefficients (16 registers of 30 bits) and D_i dealyline (16 registers of 8 bits), assuming a 99% reliability (ER = 1%). This means that the behavior of the filter is considered correct if, regardless of the SEU fluence suffered by the application, the number of cycles with a wrong output does not exceed a 1% of the total simulation time.
Several campaigns of 1.000 SEUs, with 500.000 simulation cycles, have been performed on the circuit. In these conditions, the methodology has to:

- Detect possible failures in the TMR protection.
- Avoid unnecessary area overhead due to the protection of non-sensitive nodes.

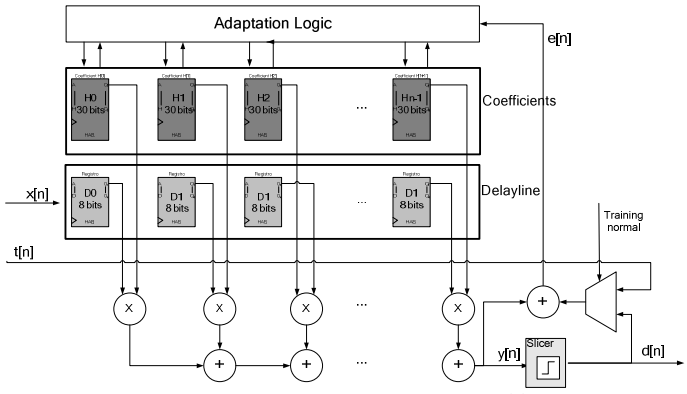

Fig. 2: Case study: Feed Forward Equalizer. * More sensitive FF, * Less sensitive FF

The methodology has started working on the full TMR version and the results after this process are:

- Firstly, the system has proved to be well protected because no errors have been transmitted to the output. This means that the full TMR structure has been well implemented.
- Secondly, an excessive area overhead caused by the full TMR protection applied to the delay line registers has been detected. This means that for the required reliability (99%), triplicating the delay line registers is unnecessary, because the Error Rate that they produce is less than the allowed 1% for the environment of the problem.

Therefore, registers in the delay line are not considered a risk to the system for the given reliability constraint and SEU fluence. Thus, they are labeled as non-sensitive nodes, as shown in Figure 2 (dark grey coefficients are more sensitive than light grey delay line). The results of the methodology in terms of area saved can be observed in Table 1.

TABLE I: AREA SAVINGS EXPRESED IN NUMBER OF FFS

Demanded reliability 99%	**Number of tripled FFs**	**Reduction**
Full TMR	608x3	0.0 %
Optimization	480x3	21.1 %

IV. CONCLUSIONS AND FUTURE WORK

In this paper, a novel methodology to verify and optimize TMR implementations has been presented. The benefits of applying the presented technique are the following:

- Given a TMR protection, the methodology verifies whether it meets the reliability constraints or there is an implementation problem in the protection.
- Given a TMR protection that already meets the reliability constraint, the methodology tries to reduce the number of tripled registers in order to reduce the area cost, while still meeting the constraints.

The next steps will focus on the analysis of other complex circuits which can be studied in order to verify and optimize their protections, and methods that can speed up the methodology.

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